Cell-Based Variable-Gain Amplifiers With Accurate dB-Linear Characteristic in 0.18 μm CMOS Technology

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Abstract—A simple and robust “cell-based” method is presented for the design of variable-gain amplifiers (VGAs). The proposed unit cell utilizes a unique gain compensation method and achieves accurate dB-linear characteristic across a wide tuning range with low power consumption and wide bandwidth. Several such highly dB-linear unit cells can be cascaded to provide the required gain range for a VGA. To prove the concept, single-cell, 5-cell, 10-cell and 15-cell reconfigurable VGAs were fabricated in a standard 0.18 μm CMOS technology. The measurement results show that the 10-cell VGA achieves a gain range of 38.6 dB with less than 0.19 dB gain error. The 15-cell VGA can either be used as reconfigurable VGA for analog control voltage or tunable PGA for digital control stream, with the flexibility of scaling gain range, gain error/step and power consumption. For the VGA at highest gain setting, it consumes 1.12 mW and achieves a gain range of 56 dB, gain error less than 0.3 dB.

Index Terms—Cell based, CMOS variable gain amplifier, dB-linear, gain compensation, low power, power scalable, programmable gain amplifier, reconfigurable.

I. INTRODUCTION

The variable-gain amplifier (VGA), or programmable-gain amplifier (PGA), is one of the critical building blocks of a transceiver. A VGA is widely used to provide a fixed output power for different input signals to improve the transceiver’s dynamic range [1]. VGAs are tuned continuously by analog control signals, whereas PGAs are tuned discretely by digital control signals. Although the design specifications of a VGA/PGA can vary significantly in terms of bandwidth, power consumption, noise and large-signal linearity for different applications, a common specification of the VGA/PGA is to accurately realize the dB-linear characteristic. To achieve this, PGAs utilizing feedback resistor arrays as well as switches are adopted for wireless communication receiver designs [2]–[5]. However, there are several drawbacks for those designs. First of all, numerous resistors and switches must be used when a small gain step is required. As a result, it occupies a large die area. Secondly, the frequency response using PGAs is usually not high due to the nature of the closed-loop structure. Finally, the gain control of PGAs is implemented at the digital baseband rather than at the analog front-end, which may have a latency issue depending on the targeted application. Therefore, extensive research has been done on the design of accurate dB-linear VGAs [6]–[26]. To achieve accurate dB-linear characteristic, the implementation of an exponential function is required. Although it is natural to design an accurate dB-linear VGA in bipolar technology due to its intrinsic exponential characteristic [3], [6], it is better implemented in a standard CMOS technology so that the cost of integration can be low. In general, due to the linear and square characteristic of the MOSFET itself, only the first-order and second-order terms of the Taylor’s series of the exponential function are realized. The omitted high-order terms are the major sources for the dB-linear gain error. When small gain error and good accuracy is required, additional circuits need to be added to approximate the high-order terms of the exponential function, leading to higher power consumption and smaller bandwidth. In short, the motivation of VGA design is driven by the requirements for better dB-linear accuracy, wider bandwidth and lower power consumption.

In this paper, a novel “cell-based” design method is presented to minimize the dB-linear gain error. Based on this method, a unique structure of the unit cell is proposed, which uses a combination of nMOS and pMOS transistors as active loads for gain compensation. The dB-linear gain control is simply realized by tuning the body bias voltage of the pMOS transistors and no additional V-I convertor is required to generate the exponential-like function. The proposed “cell-based” method also allows multiple cells to be cascaded while the overall performance in terms of dB-linear gain error, power consumption as well as bandwidth is still comparable to other previously published designs.

The remainder of this paper is organized as follows. In Section II, state-of-the-art dB-linear VGAs are summarized as benchmarks. The concept of the “cell-based” topology, the unit cell with unique gain compensation method and multiple-cell VGAs are introduced in Section III. The measurement results of the designed dB-linear VGAs are summarized in Section IV. Finally, the conclusion is presented in Section V.
II. STATE-OF-THE-ART VGA WITH DB-LINEAR CHARACTERISTIC

Designing a VGA to meet all the requirements of accurate dB-linear characteristic, large voltage-gain range, low power, low noise, wide bandwidth, and high large-signal linearity is in all likelihood impossible. Several design trade-offs must be taken into account to meet the different system specifications. In this section, some of the classical design techniques from previously presented CMOS dB-linear VGAs are discussed.

In general, the design of a CMOS-based analog VGA with accurate dB-linear gain characteristic is realized by the circuit implementations of pseudo-exponential or Taylor’s series approximation functions [16]–[21]. A typical one is shown below:

\[
\frac{1 + x}{1 - x} \quad (1)
\]

Based on the approximation in (1), less than 15 dB of dB-linear gain range with a gain error of less than 0.5 dB [16], [17] can be achieved.

Although the voltage-gain range of the VGA can be extended by cascading several stages of the VGA cell, the gain error of such a VGA can deteriorate significantly. To increase the voltage-gain range of the VGA, there are several variations of a pseudo-exponential model for approximating the exponential gain control mechanism as presented in [7]–[15]; a typical one is given below [13]:

\[
\frac{k + (1 + ax)^2}{k + (1 - ax)^2} \quad (2)
\]

where \( k \) is a constant. The simplified schematic for the implementation of this approximation is illustrated in Fig. 1(a). The numerator and denominator of (2) are quadratic functions of the variable \( x \). For \( k \) less than unity, the dB-linear range of (2) extends drastically and reaches its maximum value at around \( k = 0.12 \) [13]. As can be seen from Fig. 1(a), the resultant gain is given by the transconductance ratio between the input transistor and the diode-connected load, which can be controlled by varying the currents of the transconductance stages. As a result, respectable dB-linear gain range was achieved [13]. However, the bandwidth of the VGA is limited at high-gain settings [13], due to the fact that the output impedance of this structure is dominated by the transconductance of the diode-connected transistors. Moreover, two current sources are required for both the input and load stages. Thus, the power consumption is relatively higher than the one sharing the current between the input and load stages.

A current-steering VGA with an exponential control voltage circuit is another popular VGA technique [18], [20], [24], which...
also provides a large voltage-gain range. This technique is illustrated in Fig. 1(b). Due to the square-law characteristic of a MOS device, an exponential control generator is required. Moreover, any noise on the control voltage will be coupled to the output node.

Recently, a novel pseudo-exponential approximation is proposed in [15]. By cascading several linear functions, a high-order pseudo-exponential approximation can be realized, as shown below:

\[ e^x \approx \left(1 + \frac{x}{n}\right)^n \]  

where \( n \) is the number of cascaded linear terms. The simplified schematic is shown in Fig. 1(c). In [15], three stages are cascaded to achieve a voltage-gain range of 50 dB with a gain error of less than 0.5 dB. Although the implementation of a linear function in CMOS can be realized by biasing the transistor in triode region, the bandwidth of this structure is relatively small. It is mainly due to the fact that the voltage-gain range of the VGA is controlled by the slope of the linear function. In order to have a reasonable voltage-gain range, a large transistor needs to be used at the input. Consequently, the bandwidth of the presented VGA is limited by the parasitic capacitance. Another drawback of this structure is that devices with different threshold voltages may be required to assist in the implementation of the linear function, which may not be available for standard CMOS technology.

In contrast to the topologies discussed above, a closed-loop topology can be used. A VGA based on a differential ramp generator is presented in [23], and the simplified schematic is shown in Fig. 1(d). Utilizing a differential ramp generator, the feedback resistance can be gradually changed so that continuous gain tuning is achieved without implementing any pseudo-exponential function. By adopting a high-gain amplifier, the large-signal linearity degradation caused by the large signal swing at the inputs of the VGA is reduced, which helps to improve the large-signal linearity of the VGA. However, the bandwidth of the VGA may be limited due to the closed-loop topology. In addition, a large number of ramps are required to achieve continuous gain tuning, which increases the area and layout complexity.

Among the previously published works, the VGA’s gain error presented in [15] of less than 0.5 dB, or 1% of the voltage-gain range, is the lowest reported so far in the literature. However, the limited bandwidth and the small control voltage range make the design inappropriate for certain applications, where high frequency and low power are required. To further reduce the gain error as well as to increase the bandwidth, a simple and robust “cell-based” VGA design method will be presented in the subsequent sections.

III. DESIGN OF “CELL-BASED” VGAS WITH ACCURATE dB-LINEAR CHARACTERISTIC

Conventionally, a VGA is realized in a single stage, or by cascading only two or three stages. Cascading too many stages has several difficulties, such as high power consumption, large die area and limited bandwidth. In particular, the gain error requirement for a single-stage amplifier is very crucial, because overall gain error of a VGA will be accumulated when cascading many stages. Thus, the conventional designs are primarily focused on how to increase the dB-linear voltage-gain range of a single-stage VGA so that the number of single-stage amplifiers cascaded can be minimized. In contrast, a novel design method is proposed in this section. The simplified block diagram of the proposed VGA is shown in Fig. 1(e). Instead of focusing on how to increase the dB-linear voltage-gain range of a single-stage amplifier, our primary goal is focused on how to design a unit cell with minimized gain error and power consumption. Consequently, several of such unit cells can be cascaded to provide the required dB-linear gain range without consuming too much power. To differentiate our proposed design method with the conventional cascaded designs, we named our design as a “cell-based” method. The advantage of “cell-based” VGA design is that the number of unit cells to be cascaded can be chosen according to the system requirements. No additional circuitry, such as differential ramp or exponential generators, is required. Moreover, a reconfigurable approach, by means of a digital control, can be implemented based on the unit cell. As a result, multiple application standards can be satisfied with options for wide voltage-gain range, small gain error or low power consumption.

However, design of such unit cell is very challenging. First of all, a reasonably large control voltage range is required, as a single voltage source will be used to control the overall gain of a VGA. If the control voltage range is small, although the performance of a unit cell will not be significantly affected, the overall gain of the VGA may be very sensitive to the control voltage variation. Secondly, the gain error of a unit cell needs to be extremely small so that the accumulated gain error is still within a reasonable range. For example, if the overall gain error of a 10-cell VGA needs to be less than 0.5 dB, then the gain error of the unit cell needs to be less than 0.05 dB. Finally, the power consumption as well as area of a unit cell needs to be minimized. Otherwise, the total power consumption and the die area will be enormous. Therefore, a simple structure is preferred for the unit cell implementation. Moreover, using a simple structure to implement the unit cell also helps to maintain a wide bandwidth for the overall cascaded VGA.

A. Design of an Extremely Accurate dB-Linear Unit Cell With Unique Gain Compensation Method

The schematic of the unit cell with gain compensation is shown in Fig. 2. To compensate the gain error, both diode-connected nMOS transistors, \( M_1 \) and \( M_2 \), and diode-connected pMOS transistors \( M_3 \) and \( M_4 \) are used as active loads. Moreover, the body nodes of \( M_3 \) and \( M_4 \) are used for continuous gain tuning. \( M_7 \) and \( M_8 \) serve as the inputs of the differential pair with input signal applied at their gate nodes and output signal taken from their drain nodes. \( M_7 \) is the current source providing the bias conditions. By inspection, the overall differential voltage gain is derived as:

\[ A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4}} \]
where $g_m$ is the transconductance of the respective transistor. The current relationship can be expressed as (assuming all currents are flowing downwards):

$$I_{DS,5,6} = I_{DS,1,2} + I_{DS,3,4}. \quad (5)$$

As the currents flowing through $M_5$ and $M_6$ are constant, $g_{m,5,6}$ is constant throughout the whole tuning range and $\Delta g_{m,5,6} = 0$. Thus (4) with the change in $g_m$ represented as $\Delta g_m$ can be rewritten as:

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \Delta g_{m,1,2} + \Delta g_{m,3,4}}. \quad (6)$$

In this design, the nMOS load $M_1$ and $M_2$, are biased in the subthreshold region, while the pMOS load $M_3$ and $M_4$ are biased in the saturation region. Thus the change in their transconductance, $\Delta g_{m,1,2}$ and $\Delta g_{m,3,4}$ can be expressed as:

$$\Delta g_{m,1,2} = \frac{2I_{DS,1,2}}{nV_T} \quad (7)$$

$$\Delta g_{m,3,4} = \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left( \frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right) \quad (8)$$

Substituting (7) and (8) into (6) leads to (9), shown at the bottom of the page, where $V_{OV,3,4}$ is the overdrive voltage and $V_{OV,3,4} = V_{GS,3,4} - V_{TH,3,4}$. As the total current remains unchanged, $\Delta I_{DS,1,2} = -\Delta I_{DS,3,4}$, and (9) is rewritten as (10), also shown at the bottom of the page.

The basic pMOS I-V equations for $M_3$ and $M_4$ with channel-length modulation neglected can be written as:

$$I_{DS,3,4} = \frac{1}{2} K_P V_{OV,3,4}^2 = \frac{1}{2} K_P (V_{GS,3,4} - V_{TH,3,4})^2 \quad (11)$$

where

$$K_P = \mu P C_{ox} \left( \frac{W}{L} \right)_{3,4}. \quad (12)$$

As the percentage change in $I_{DS,3,4}$ is larger than the percentage change in $V_{OV,3,4}$ due to their quadratic relationship as shown in (11) and of the same polarity, as well as $V_{GS,3,4} + \Delta V_{OV,3,4}$ is always much larger than $nV_T$ due to their different operation region, the following inequality is established:

$$\left| \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left( \frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right) \right| < \left| \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \right| \ll \frac{2I_{DS,3,4}}{nV_T}. \quad (13)$$

Thus the last term in the denominator of (10) can be ignored and the gain can be approximated as:

$$A_v \approx \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} - \frac{2I_{DS,3,4}}{nV_T}}. \quad (14)$$

The threshold voltage with body effect considered can be expressed as follows:

$$V_{TH,3,4} = V_{TH0} - \gamma P \left( \sqrt{V_{SB,3,4} + 2\varphi_F} - \sqrt{2\varphi_F} \right) \quad (15)$$

where $V_{TH0}$ is the threshold voltage without considering body effect, $\gamma_P$ and $\varphi_F$ are body-effect related parameters.

As long as the nMOS load transistors $M_1$ and $M_2$ are large enough and stays in subthreshold region, the change in $V_{GS,3,4} = -V_{GS,3,4}$ can be ignored and $\Delta I_{DS,3,4}$ only depends on the change in $V_{TH,3,4}$. With (15) substituted into (11) and $V_{GS,3,4}$ constant, $\Delta I_{DS,3,4}$ can be obtained by taking the derivative of $I_{DS,3,4}$ w.r.t. $V_{SB,3,4}$ multiplied by $\Delta V_{SB,3,4}$:

$$\Delta I_{DS,3,4} = \frac{0.5\gamma_P \star \sqrt{2I_{DS,3,4}K_P}}{\sqrt{V_{SB,3,4} + 2\varphi_F}} \Delta V_{SB,3,4}. \quad (16)$$

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \frac{2I_{DS,1,2}}{nV_T} + \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left( \frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right)} \quad (9)$$

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} - \frac{2I_{DS,3,4}}{nV_T} + \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left( \frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right)} \quad (10)$$
The range for $V_{SB,3,4}$ is from 0 V to 0.6 V due to physical limitations. A negative $V_{SB,3,4}$ requires a voltage higher than $V_{DD}$ and a separate source must be used, while $V_{SB,3,4} > 0.6$ V will forward bias the body-source junction, leading to observable body current. A center $V_{SB,3,4}$ of 0.3 V is used and $\Delta V_{SB,3,4}$ is within ±0.3 V. All other constant terms are calculated at $V_{SB,3,4} = 0.3$ V. The calculated relationship between $V_{SB,3,4}$, $\Delta I_{DS,3,4}$ and the overall voltage gain in dB is plotted in Fig. 3. As can be seen from Fig. 3, $\Delta I_{DS,3,4}$ vs. $V_{SB,3,4}$ is plotted based on (16) and forms a convex relationship, and the gain vs. $\Delta I_{DS,3,4}$ is plotted based on (14) and forms a concave relationship. Although these two curves alone are not dB-linear, the resultant relationship of gain vs. $V_{SB,3,4}$ is compensated to be dB-linear. The size of the nMOS load transistors and the pMOS load transistors should be selected properly for the best gain compensation.

The selection for the sizes of pMOS transistors, $M_3$ and $M_4$ to satisfy all the above-mentioned equations is critical. When other conditions hold, varying the sizes of $M_2$ and $M_4$ changes $K_p$, as it is related to the $W/L$ ratio as shown in (12), and thus to $I_{DS,3,4}$ according to (11). For a smaller device, both $K_p$ and $I_{DS,3,4}$ are smaller, resulting in a smaller $\Delta I_{DS,3,4}$ and a smaller voltage-gain range. To increase the voltage-gain range, larger device can be used. If a larger device is selected, $I_{DS,3,4}$ are larger, resulting in a larger $\Delta I_{DS,3,4}$ and voltage-gain range. As long as the above-mentioned equations still hold, the larger device is used, the larger voltage-gain can be achieved. However, further increasing the size of the device is undesirable, as $M_3$ and $M_4$ cannot draw more current and $\Delta I_{DS,3,4}$ is almost flat, leading to curvy gain characteristic and significant gain error. As shown in Fig. 4, the width of the pMOS transistor is selected to be 2 $\mu$m.

On the other hand, the selection for the size of nMOS transistors, $M_1$ and $M_2$ is also important and is as follows. As can be seen from Fig. 5, as long as the nMOS transistor is large enough to be biased in the subthreshold region, the accurate dB-linear characteristic can be achieved. Following the same discussion, that for a large nMOS transistor, the current distribution between the pMOS load and the nMOS load will follow the former, as the current in a subthreshold nMOS transistor can vary significantly and the change in $V_{GS,1,2}$ can be ignored. Thus, for large nMOS transistors, $\Delta I_{DS,3,4}$ will follow the same trend and the resultant gain is always dB-linear with a large voltage-gain range. For a small nMOS transistor, sharing $\Delta I_{DS,3,4}$ will drive the nMOS transistors out of the subthreshold region, with a trend of decreasing $\Delta I_{DS,3,4}$. Thus the gain characteristic is curvy with a smaller voltage-gain range. In this design, an optimized nMOS transistor width of 4.5 $\mu$m is selected.

Simulation results showed that the above mentioned unit cell utilizing this unique gain compensation method exhibits low power consumption, small area and large bandwidth. It can also achieve an extremely small gain error of 0.015 dB over a voltage-gain range of 4 dB, or 0.4% of the gain range.

B. Design of a 10-Cell VGA With Temperature Variations

Using the proposed unit cell, a 10-cell VGA can be simply implemented by directly cascading 10 unit cells. The simplified block diagram of the presented 10-cell VGA is shown in Fig. 6. From a practical design point of view, the mismatch of
transistors should be taken into account. As shown in Figs. 4 and 5, the unit cell has a voltage-gain range of 4 dB. Therefore, 10 cells should achieve a dB-linear voltage-gain range of 40 dB. However, directly cascading 10 cells may lead to a DC-offset issue at high gain settings. Thus, two approaches, with and without DC-offset cancellation are implemented. Although both AC-coupling [24] and DC-feedback loop can be used to eliminate the DC-offset issue, AC-coupling is chosen for its simplicity. To demonstrate the feasibility of the proposed method, AC-coupling circuitry is inserted between every two cells to guarantee the overall performance.

The simulated dB-linear characteristic of the designed 10-cell VGA in terms of dB-linear gain range and gain error with three typical temperatures, 20°C, 27°C and 80°C, are shown in Fig. 7(a) and (b), respectively. As can be seen from Fig. 7(a), the temperature variation does affect the dB-linear gain range. As the temperature goes higher, the dB-linear gain range is reduced. On the other hand, the dB-linear gain error is almost insensitive to temperature variations, as illustrated in Fig. 7(b).

C. Design Consideration for “Skew” Process Variations

To further demonstrate the robustness and usefulness of the presented approach, the impact of process variations on the dB-linear characteristic of the 10-cell VGA is investigated. For simplicity, in the previous sections, we used “self-biased” nMOS transistors at the load so that no additional bias voltage is required. Since both the nMOS and pMOS transistors are used in the design, the parameters of both transistors may not have identical tendency with respect to process variations, despite that they work well within a wide range of temperature.

To guarantee the performance under “skew” case, such as SF and FS corners, the unit cell can be modified as shown in Fig. 8. In order to weight and divert the current between the nMOS and pMOS devices of the presented unit cell, a one-time calibration voltage $V_{CAL}$ at the gate nodes of the nMOS transistors $M_1$ and $M_2$ is introduced. The value of such calibration voltage can be selected according to the results of the process control monitoring (PCM) on the same reticle. In contrast to the circuit presented in Fig. 2 where $V_{CAL} = V_{DD}$, this one-time calibration voltage can be varied to force the nMOS device to operate in subthreshold region. With an appropriate selection on $V_{CAL}$, the dB-linear gain characteristic of the 10-cell VGA, as shown in Fig. 9, can be tuned insensitive to process variations.

D. Design of a 15-Cell Reconfigurable VGA or Tunable PGA

The presented “cell-based” method can be used for a cascaded VGA design, as well as to design a reconfigurable VGA which can also be used as a tunable PGA. The simplified block diagram of the designed 15-cell reconfigurable VGA consisting of 0 to 15 cells is shown in Fig. 10. As can be seen from Fig. 10, 15 VGA cells are cascaded and controlled by a 4-bit digital signal so that gain reconfigurability and power scalability can be demonstrated. Again, AC-coupling circuitry is inserted between every two cells. The power consumption is stepped from 0 to 15 times that of the unit cell depending on the digital bits, and it consumes 0.62 mA at the highest gain setting. The simulated gain of the VGA as a function of both analog control voltage and
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IV. FABRICATION AND MEASUREMENT

To verify the proposed design method, the VGAs shown in Figs. 6 and 10 were fabricated in Globalfoundries’ 0.18 μm CMOS technology. Other than that, a single-cell and a 5-cell VGA without any DC-offset cancellation circuitry were also fabricated for evaluation purpose. The on-wafer measurement was performed using an Agilent E8364B vector network analyzer, which operates from 10 MHz to 50 GHz. In order to drive the 50 Ω vector network analyzer, a differential buffer is included after each VGA and is also fabricated separately for de-embedding purpose. The buffer is measured to have 16 dB of attenuation at all frequency. In the following discussion, the attenuation of the buffer is always de-embedded from the measurement, so that the performance of the “core” circuit can be effectively reflected. Moreover, a fixed 20 MHz signal is used for all of the dB-linear gain characterization, output 1 dB compression (\(P_{1\text{dB}}\)) and input-referred noise (IRN) measurements.

The measured and simulated dB-linear gain characteristic in terms of gain range and gain error of the single-cell VGA are presented in Fig. 12(a) and (b), respectively. As illustrated in Fig. 12(a), a gain range of 4 dB is achieved from a unit cell. The measured and simulated gain error of the unit cell can be seen from Fig. 12(b). The measured gain error is 0.08 dB, which is much larger than the simulated 0.015 dB. Such discrepancy between the simulation and measurement is mainly due to the limited equipment accuracy. A more reasonable comparison between simulation and measurement in terms of gain error will be indirectly presented based on one tenth that of the 10-cell VGA. The power consumption of the single-cell VGA is only 41 μA under a 1.8 V power supply.

Fig. 13(a) and (b) shows the measured and simulated dB-linear gain characteristic of the 10-cell VGA with AC coupling circuitry. A gain range of 38.6 dB is achieved while \(V_{\text{CTRL}}\) is swept from 1.225 V to 1.8 V. Within this gain range, the measured gain error is 0.19 dB (0.49% of voltage-gain range), which is reasonably close to the simulated value of 0.17 dB. The gain error of unit cell is thus derived as 0.019 dB, which is also close to the simulated result in Fig. 12(b). The power consumption for this VGA core is 412 μA, which is as expected ten times that of the unit cell.

Fig. 14(a) and (b) shows the measured and simulated gain range and gain error of the 15-cell reconfigurable VGA. A maximum gain range of 63 dB is achieved while \(V_{\text{CTRL}}\) is swept from 1.2 V to 1.8 V. The measured gain error is 0.3 dB with the
dB-linear gain range being 56 dB (0.54%), which is also quite close to the simulated value of 0.26 dB. The power consumption for this VGA core is 620 μA at its highest gain setting.

Figs. 15–17 show the measured frequency responses of the fabricated VGAs under various $V_{CTRL}$ values. The impact of the parasitic capacitance on the frequency response of the designed VGA is negligible. The measured results are almost identical to the post-layout simulation. As can be seen from the figures, the bandwidth for single-cell, 10-cell, and 15-cell reconfigurable VGAs are 284 MHz, 149 MHz, and 63.5 MHz, respectively, under the highest gain setting. It can be seen from Figs. 15–17 that the bandwidth of the VGA is reduced while more cells are cascaded. Due to the simple gain compensation structure, the bandwidth of the unit cell is relatively wide, thus the resultant bandwidth of the cascaded VGA is still reasonable for many applications.

As previously discussed, the mismatch of transistors should be taken into account to evaluate the DC-offset issue. Therefore, the 10-cell VGA without any AC coupling circuitry is also fabricated. It exhibits DC-offset problem at high gain settings, and the voltage-gain is dB-linear only for the $V_{CTRL}$ between 1.8 V and 1.4 V.

To further evaluate the DC-offset issue, the fabricated 5-cell VGA is also measured. The measurement result shows that the 5-cell VGA can produce around 20 dB of voltage-gain range and no DC-offset problem is observed. As each unit cell is DC-coupled to each other without having any AC-coupling circuitry, the core of 5-cell VGA only occupies an area of 0.0007 mm² ($23 \times 32 \mu m²$), which indicates that if more compactness is required, the AC-coupling circuitry can be inserted between every five cells. The gain error and power consumption of 5-cell VGA are around half of that for the 10-cell VGA as the cascaded structure is the same.

The measured output $P_{1dB}$ and IRN for the 10-cell VGA is shown in Fig. 18. The measured output $P_{1dB}$ is around $-3$ dBm for the highest gain setting, while the IRN is around $10.6$ nV/$\sqrt{Hz}$.

Fig. 19 shows the die photos of the fabricated VGAs. It can be seen that the unit cell or even 10 cells directly cascaded is compact and the main area-consuming block is the AC-coupling circuitry. The VGA core is very compact and much smaller
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Fig. 14. Gain characteristic of the 15-cell reconfigurable VGA: (a) dB-linear gain range, (b) gain error.

Fig. 15. Measured frequency response of the single-cell VGA.

Fig. 16. Measured frequency response of the 10-cell VGA.

Fig. 17. Measured frequency response of the 15-cell reconfigurable VGA.

Fig. 18. Measured output $P_{1dB}$ and IRN vs. $V_{CTRL}$.

than other published VGAs. Even with the AC-coupling circuitry, the size is still comparable to other published VGAs. A

summary and comparisons between the proposed VGAs with other state-of-the-art designs are given in Table I.

V. CONCLUSION

In this paper, a simple and robust “cell-based” method is presented for the design of VGAs with accurate dB-linear...
The presented unit cell achieved extremely accurate dB-linear characteristic across a wide tuning range, based on a unique gain compensation method with a combination of subthreshold nMOS and body-tuned pMOS transistors as active loads. Several such highly dB-linear unit cells can be cascaded to provide the required gain range for a VGA while achieving low power consumption and wide bandwidth. Single-cell, 5-cell, 10-cell, and 15-cell reconfigurable VGAs were fabricated in a standard 0.18 μm CMOS technology. The measurements show that the 10-cell VGA achieves a gain range of 38.6 dB with less than 0.19 dB gain error or 0.49%. The 15-cell VGA can either be used as reconfigurable VGA for analog control voltage or tunable PGA for digital control stream, with the flexibility of scaling gain range, gain error/step and power consumption. For the VGA at highest gain setting, it consumes 1.12 mW and achieves a gain range of 56 dB, gain error less than 0.3 dB or 0.54%. Among the previously published works in the literature, the performance of the presented “cell-based” VGA is very competitive in terms of dB-linear gain error. Therefore, the presented “cell-based” designs may be suitable for many applications, where low power and high frequency are required.

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