Final Year Project Proposal 1

Project Title:
Cu metallization removal for failure analysis of ICs

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentors:
Ms Katherine Kor
Dr Liu Qing

Description:
In recent years, even though a defect is well understood electrically, an image of the anomaly is needed to verify the defect location. However, ICs have more than one metallization layer. It is impossible to view the many types of defects without first removing the overlying layers. The inter-dielectric layer can be removed by RIE or chemical etch. However, in some cases, the removal of one layer can act as an in-situ decoration of another layer, masking the defect. In this situation, a proper removal method is required.

In this project, a 65 nm chip with Cu metallization will be studied. Different Cu metallization removal methods will be investigated, such as mechanical etching by polishing, chemical etching and dry etching. Meanwhile, inter-metal dielectric removal techniques will also be investigated. The main focus is to avoid damage to the underlying layers when removing the current layer.

Methodology:
Focus Ion Beam (FIB) will be used to study the thicknesses of the layer stacks of the 65 nm Cu chip. Then, the Cu chip will be delayered by the different techniques. Optical images of the Cu chip will be captured during the delayering process. Meanwhile, SEM with EDX is required to verify the materials and morphology.

Equipment:
SEM, Polisher, RIE (NTU)

Remarks:
As delayering is a delicate process, this may require much patience from student. Etching also requires dealing with chemicals such as acids.
Final Year Project Proposal 2

Project Title:
Package decapsulation for failure analysis of ICs

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentors:
Dr Liu Qing
Ms Katherine Kor

Description:
Decapsulation is a failure analysis step carried out to open a package in order to facilitate the inspection, electrical examination, or chemical analysis of the internal features of the package. Several decapsulation methods are available, such as jet etching, total package removal, manual cavity etching. Among these methods, jet etching is a semi-automated version of chemical decapsulation. Fuming nitric acid and sulfuric acid or a mixture of the two acids are used. With the advancement of technology, modern chips are fabricated with more complicated types of packages. Proper decapsulation methods are needed.

In this project, several types of packages will be studied. Different decapsulation methods will be investigated, such as laser decapsulation, semi-automatic acid decapsulation, manual acid decapsulation, or mechanical decapsulation. The main focus is to avoid the damage to the chips when removing the packages.

Methodology:
The microelectronic packages will be decapsulated by different techniques. Optical images of the decapsulated micro-chips will be captured after the decapsulation process.

Equipment:
Optical Microscope, Polisher, RIE (NTU)

Remarks:
Decapsulation will require some dealing with acids.
Final Year Project Proposal 3

Project Title:
Mechanical reliability of electronic packages under adverse environment

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Mr Eric Phua Jian Rong

Description:
Ruggedized electronics is crucial to ensure continuous operation during drilling (LWD, MWD) operations in subsea drilling environments. High temperature, pressure and even changes in electrochemistry with deployment of these packages in drilling tools posed a challenge to their survivability. In this project, various modes of mechanical testing are required to mimic the adverse environmental conditions on electronic packages.

Methodology:
Real time operation conditions such as high temperature, pressure and vibration would be applied on electronic packages. These packages are then tested for mechanical reliability and electrical reliability. Nanoindentation, Vickers hardness and SEM techniques are used to determine the properties of existing or new materials.

Equipment:
Furnace, Vickers hardness, Indentation, Scanning Electron Microscopy, Probe Station (NTU)
Die Shear Test (Institute of Microelectronics)

Remarks:
Student may require to carry out some testing in Institute of Microelectronics.
Final Year Project Proposal 4

Project Title:
High temperature polymeric gap fill materials for electronic packages

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Mr Eric Phua Jian Rong

Description:
Ruggedized electronics is crucial to ensure continuous operation during drilling (LWD, MWD) operations in subsea drilling environments. High temperature, pressure and even changes in electrochemistry with deployment of these packages in drilling tools posed a challenge to their survivability. In this project, various modes of characterization are required to identify suitable high temperature polymeric gap fill materials in electronic packages.

Methodology:
High temperature polymeric materials would be used in this case for filling up packages. Prior to that, selected polymers would be characterized to check their suitability for the environments which they would be placed in. Compatible polymers identified would be placed into actual packages which would subsequently undergo electrical and mechanical reliability tests.

Equipment:
DSC, TGA, DMA, SEM (NTU)
CSAM (Institute of Microelectronics)

Remarks:
Student may require to carry out some testing in Institute of Microelectronics.
Final Year Project Proposal 5

Project Title:
Development of non-destructive thin metal film adhesion (by Study of relation between electrical test and mechanical test properties of thin film)

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Dr I Made Riko

Description:
Increasing fuel demand and ever scarcity of the natural resource such as oil, had driven efforts to find new oil reserve deep in earth mantel. Deep earth exploration requires a much more reliable instrumentation and sensors that can survive extreme pressure and temperature such as 2000 atm and 300°C, respectively. Ceramics had been identified as suitable materials that could give reasonable protection for sensitive electronic device from extreme environment. However, metal interconnects highly suffer at those extreme condition.

Survey of suitable materials and materials composition typically involve slow, tedious and destructive mechanical tests to quantify metal to ceramics adhesion. Thus, there is a need to develop a faster, reliable and non-destructive method to quantify metal adhesion to ceramics surface.

In this project, we will try to find an empirical relation between electrical properties of metal thin film with mechanical test results, i.e Scratch Test, Pull Test, Chevron Pull Test.

Methodology:
Simple test structure fabrication:
 a. Shadow mask construction on ceramics surface by adhesive thermal tape.
 b. Thin metal film deposition on ceramics substrate by physical vapor deposition.
 c. Film thickness characterization
 d. Electrical properties measurement, resistance, resistivity
 e. Mechanical scratch test
 f. Chevron test
 g. Microscopic characterization

Equipment:
Sputtering System, Sintering Furnace, Probe station, SEM/EDX, Profilometer, Shimadzu XRD (NTU)
Remarks (from mentor):
The student is expected to

1. Independently gather, **summarize and simplify** necessary information for this project, may that from literature, news or interview.
2. Independently able to **identify**, obtain access and get trained on equipment and instruments for necessary fabrication and characterization in MSE, based on the information obtained from literature review.
3. Independently able to design and execute and **documents** experiments procedure based information gathered from literature and MSE’s available equipment and instrument.
Final Year Project Proposal 6

Project Title:
Transient liquid phase (TLP) die attach for high-temperature devices

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Dr Ahmed Sharif

Description:
Some specialized microelectronics (e.g. application in automotive, geothermal, and aerospace systems) need to operate at high temperatures (>300°C), which places severe demands on the device packages. In microelectronic systems, die attach is an important step in the packaging of semiconductor devices. Transient liquid phase (TLP) bonding is one approach to form a high-temperature die bonds. In this bonding process, the integrity of the bond is enhanced by the formation of a liquid phase, yet the bond is able to withstand an operating temperature above the bonding temperature once solidification is complete. Different types of TLP based die attach will be investigated to find a suitable combination for the ceramic substrate and the device.

Methodology:
Both the physical vapor deposition (PVD) and powder metallurgy route will be utilized to form the bonding structure between the device and substrate and as well on the Cu substrates. The bonding will be done inside a furnace with some pressure. Then the mechanical, electrical and microstructural characterization will be done to evaluate the bond quality.

Equipment:
Bonding setup, Furnace, Scanning Electron Microscopy, Universal Tester, Micro/Nano Hardness Tester, DSC, XRD, Probe Station (NTU)

Remarks:
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Final Year Project Proposal 7

Project Title: Study on the adhesion and reliability of high temperature plastic encapsulants

Supervisor: Assoc. Prof. Gan Chee Lip

Mentor: Dr Ahmed Sharif

Description: One of the major applications of polymers in electrical and electronic industrials is for use as encapsulants of electrical circuits and electronic devices. Recent developments in semiconductor and electronic packages require molding compounds possessing superior properties of high temperature stability, low shrinking stress, low dielectric constant, and low thermal expansion coefficients. This project will be dealing with the different types of potential thermoplastic and/or thermoset polymers for enhanced temperature stability and as well as better adhesion with both the ceramics and the metals.

Methodology: The adhesion quality of the high temperature polymers with both the ceramics and the metals will be studied and evaluated. The optimization of the bonding/encapsulation parameters will be executed. Microstructure characterization will be performed using advance microscopy techniques. Reliability analysis will be performed using high-temperature storage, high-humidity storage, pressure cooker test, hermeticity test and shear strength measurements.

Equipment: Adhesion setup, Oven, Scanning Electron Microscopy (SEM) /EDX, Universal Tester, Micro/Nano Hardness Tester, DSC/ TGA, XRD, FTIR (NTU)

Remarks: Student may require to carry out some testing in Institute of Microelectronics.
Final Year Project Proposal 8

Project Title:
Performance evaluation of a tailor-made glass frit die attach/hermetic sealing for high temperature application

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Dr Ahmed Sharif

Description:
Glass frit bonding is pattern-able, has excellent sealing performances with high bonding strength and has less CTE mismatch compared to ceramics and silicon. Glass frit bonding is considered as the best solution for the hermetic ceramic packages. In this project, different types of metallic/ ceramic additives will be added to the commercially available glass frit to improve its bonding property.

Methodology:
The powder metallurgy route will be utilized to form the bonding structure between the device and ceramic substrates. The bonding will be done inside a furnace with or without pressure. Then the mechanical and microstructural characterization will be done to evaluate the bond quality. Reliability analysis will be performed using high-temperature storage, high-humidity storage, hermeticity test and shear strength measurements.

Equipment:
Bonding setup, Furnace, Scanning Electron Microscopy, Universal Tester, Micro/Nano Hardness Tester, DSC/TGA, XRD (NTU)

Remarks:
Student may require to carry out some testing in Institute of Microelectronics.
Final Year Project Proposal 9

Project Title:
Compositional dependence of Sn-Zn solder on the intermetallic compound (IMC) growth kinetics with Cu at thin film scales

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Dr Wardhana Sasangka

Description:
Incorporating different elements into Sn solder has become an efficient way to control the growth rate of IMC that form with Cu film. However, which composition allows the fastest/slowest IMC growth is not yet fully understood. The existing methodology using ex-situ heating followed by cross-sectional analysis does not only suffer in accuracy but also requires rigorous effort in implementation and therefore inefficient to answer this question.

Previously, we have developed a methodology that allows fast characterization of diffusion kinetics in Cu/Sn-based bilayer system. We have used the technique to analyze Sn-In system. Understanding other material systems such as Sn-Bi and Sn-Zn will not only be useful to provide the database in literature, but also as a guideline to develop a model that relate the solder composition and IMC growth rate.

Methodology:
Cu\text{Sn}_{x}\text{Zn}_{100-x} bilayer films will be deposited on transparent glass stripes. Broad composition variation of Sn\text{Zn}_{100-x} will be produced by a combinatorial deposition. Then, these glass stripes will be annealed on a hot plate while monitoring the color change from the back of the glass stripes. Cu has an orange-ish color and transforms to shiny-white when forming IMC. The time required for color change is recorded; Cu consumption rate and therefore the IMC growth kinetics can then be deduced.

Complimentary experiments will be carried out to identify the IMC type and also microstructural evolution.

Equipment:
X-ray diffraction spectroscopy, Scanning Electron Microscopy, In house annealing setup, Sputter deposition machine, Surface Profiler (NTU)

Remarks:
This project will run in parallel with project 10.
Final Year Project Proposal 10

Project Title:
Compositional dependence of Sn-Bi solder on the intermetallic compound (IMC) growth kinetics with Cu at thin film scales

Supervisor:
Assoc. Prof. Gan Chee Lip

Mentor:
Dr Wardhana Sasangka

Description:
Incorporating different elements into Sn solder has become an efficient way to control the growth rate of IMC that form with Cu film. However, which composition allows the fastest/slowest IMC growth is not yet fully understood. The existing methodology using ex-situ heating followed by cross-sectional analysis does not only suffer in accuracy but also requires rigorous effort in implementation and therefore inefficient to answer this question.

Previously, we have developed a methodology that allows fast characterization of diffusion kinetics in Cu/Sn-based bilayer system. We have used the technique to analyze Sn-In system. Understanding other material systems such as Sn-Bi and Sn-Zn will not only be useful to provide the database in literature, but also as a guideline to develop a model that relate the solder composition and IMC growth rate.

Methodology:
Cu\text{Sn}_{x}\text{Bi}_{100-x} bilayer films will be deposited on transparent glass stripes. Broad composition variation of Sn_{x}Bi_{100-x} will be produced by a combinatorial deposition. Then, these glass stripes will be annealed on a hot plate while monitoring the color change from the back of the glass stripes. Cu has an orange-ish color and transforms to shiny-white when forming IMC. The time required for color change is recorded; Cu consumption rate and therefore the IMC growth kinetics can then be deduced.

Complimentary experiments will be carried out to identify the IMC type and also microstructural evolution.

Equipment:
X-ray diffraction spectroscopy, Scanning Electron Microscopy, In house annealing setup, Sputter deposition machine, Surface Profiler (NTU)

Remarks:
This project will run in parallel with project 9.
Final Year Project Proposal 11

Project Title:
Graphene growth through segregation method

Supervisor:
Assoc. Prof. Gan Chee Lip

Graduate Mentor:
Dr Ong Hock Guan, Steve

Description:
Graphene is a promising candidate for the use in future nanoelectronics. However, there are still some challenging areas that need to be addressed before it can be implemented commercially. One such area is the controlled growth of large area single layer graphene sheet. Currently, graphene can be synthesized by mechanical exfoliation, chemical methods, chemical vapor deposition (CVD) and segregation. Mechanical exfoliation of HOPG has produced the best quality of graphene. However, this technique can neither be scaled for mass production, nor be used to grow large sheet of graphene. Chemical methods offered ways to produce chemically converted graphene in large amount, but it lacks the control in size. CVD is able to produce large area graphene sheet with good electrical properties. However, the use of methane feedstock and many parameters needed in CVD technique increase the cost and complexity that has to be dealt with in the case of commercial production. Segregation is a simple way to achieve large area growth of graphene sheet. However, its drawback is that carbon impurity varies in different batch of metal catalyst. So, there is still a lack of a simple, cheap and scalable process to synthesize graphene for commercialization purpose in electronics fabrication.

Methodology:
The student will first optimize the type and concentration of solid carbon source to use. Poly methyl methacrylate (PMMA) will be tried out as the solid carbon source as it can be safe, cheap and easy to handle. Copper will be used as the metal catalyst as it has low carbon solubility.

Equipment:
Raman spectrometer, Scanning Electron Microscopy, Probe Station, Sputtering Machine (NTU)

Remarks: (from mentor)
Student with commitment of at least 5 hrs per week and independent abilities to research on the topic are required.