A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer With In-Phase Injection-Coupled QVCO in 65 nm CMOS Technology

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Abstract—A fully integrated 60 GHz frequency synthesizer with in-phase injection-coupled quadrature voltage-controlled oscillator (IPIC-QVCO) is proposed. Through a particular symmetrical coupling network formed by diode-connected transistors, the in-phase coupling is realized in the IPIC-QVCO, which reduces both phase noise and phase error. A compact inductor-less divider chain is designed to reduce power consumption. A self-correcting low spur charge pump is employed to reduce reference spur. A standalone 60 GHz IPIC-QVCO and a fully integrated PLL are implemented in standard 65 nm low power CMOS technology. The measurement results show that the QVCO covers a frequency range from 57.88 to 68.33 GHz while consuming 11.4 mW power from a 1.2 V supply. The phase noise of the QVCO is –92 ~ –95 dBc/Hz at 1 MHz offset. The FOM and FOMT of the QVCO are –178.1 ~ –179.7 and –182.5 ~ –184.1 dBc/Hz respectively. The tuning range of the frequency synthesizer is from 57.9 to 68.3 GHz, and the power consumption is 24.6 mW. The phase noise of the frequency synthesizer is –89.8 ~ –91.5 dBc/Hz at 1 MHz offset across the frequency band.

Index Terms—CMOS, frequency synthesizer, in-phase injection-coupled (IPIC), low phase error, low phase noise, low power, millimeter-wave, PLL, quadrature voltage-controlled oscillator (QVCO), 60 GHz.

I. INTRODUCTION

EXT-GENERATION short range high data rate wireless communication in the unlicensed 60 GHz frequency band was intensively investigated in the last decade. As defined in the 60 GHz standards, such as IEEE 802.15.3c, IEEE 802.11ad, WiGig, WirelessHD, and ECMA-387 [1]–[5], the total 9 GHz (57–66 GHz) bandwidth is divided into four 2.16 GHz channels. To achieve a higher data rate, complex modulations such as 16-QAM must be adopted, which increases the requirements of local oscillator’s (LO’s) phase noise and phase error. In recent years, it has already been demonstrated that advanced CMOS technology has the capability of realizing millimeter-wave (mm-wave) integrated circuits. CMOS implementation can reduce cost and improve yield, since RF front-end can be integrated with analog and digital baseband circuits.

Direct-conversion architecture is popular for 60 GHz transceivers because of its simple structure and fewer components [6]–[12]. Phase locked-loop (PLL) is an important block in a transceiver. Design of the wide range, low phase noise, low phase error and low power CMOS PLL for the 60 GHz direct-conversion transceiver is challenging, due to trade-offs between tuning range, phase noise, phase error, and power consumption. There are many methods for generating mm-wave quadrature LO signals, but they suffer from many problems. 1) The most common method is through a conventional mm-wave parallel quadrature voltage-controlled oscillator (P-QVCO), but its phase noise is poor [13]. 2) The method of using a divide-by-2 divider after a VCO with double LO frequency prevails in multi-GHz applications, but it is difficult to design a VCO and a divider at very high frequency. Moreover, the power consumption of this method is high. 3) If passive components such as an RC polyphase filter or quadrature hybrid coupler are used to produce quadrature signals, we usually need buffers to compensate their loss, so the power consumption is also high [6]. 4) Using an injection-locked multiplier is a good choice [14], but the disadvantages are limited locking range and intrinsic phase error due to the imbalance of the structure, or quadrature inputs are needed to overcome these two drawbacks [9].

In this work, we present a wide range, low phase noise, and low power 60 GHz quadrature PLL [15]. The simplified block diagram of the proposed PLL is shown in Fig. 1. It is an integer-N third-order charge-pump PLL with a 135 MHz reference input. The 60 GHz in-phase injection-coupled (IPIC) QVCO is proposed to reduce phase noise and phase error. Its operation frequency can cover the four required frequency spots in IEEE 802.15.3c and other compatible 60 GHz standards. The low power inductor-less frequency divider chain consists of a modified divide-by-4 dynamic current-mode logic (DCML) divider, a divide-by-4 multi-phase injection-locked frequency divider (ILFD), and a multi-modulus true-single-phase-clock (TSPC) divider. The low spur self-correcting charge pump is employed to reduce the reference spur. A standalone 60 GHz IPIC-QVCO and a fully integrated 60 GHz PLL are implemented in standard 65 nm low power CMOS technology to demonstrate our ideas. Measurement results show that the proposed IPIC-QVCO and quadrature PLL can achieve good performance with low power consumption.

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The paper is organized as follows. Section II discusses the proposed IPIC-QVCO, including architecture, analysis, and circuit design. Section III describes the frequency divider chain and charge pump design. Experimental results are provided in Section IV and conclusions are drawn in Section V.

II. IN-PHASE INJECTION-COUPLED QVCO

A. Proposed In-Phase Injection-Coupled QVCO

In general, the QVCO consists of two identical oscillators pulling each other, through coupling networks, to lock at a common frequency with quadrature phase. It is well known that in QVCO, the in-phase coupling can reduce both phase noise and phase error [16]. Many phase shifting techniques were presented to realize the in-phase coupling [16]–[21]. But their coupling networks are either RC-based or LC-based phase shifters, which are both frequency-dependent.

The in-phase coupling is realized in the proposed IPIC-QVCO by using the frequency-independent network, instead of the frequency-dependent phase shifter. In fact, the most neglected thing is that, quadrature signals always exist in a QVCO inherently. Therefore, intuitively, in-phase coupling can be realized through a particular symmetrical coupling network. Similar concepts have already been demonstrated in multiphase injection ILFDs [22]–[24]. We will prove that this concept also works in our QVCO. The schematic of the proposed QVCO is shown in Fig. 2. The two identical differential LC cross-coupled VCOs are coupled through a symmetrical coupling network. In the coupling network, each diode-connected transistor connects two oscillation nodes with phase difference, e.g., transistor $M_{C1}$ connects node $Q_+$ and node $I_+$. So the four diode-connected transistors form a symmetrical ring. As will be analyzed later, this configuration can generate in-phase injection current with the tank current.

To understand the basic concept of the in-phase coupling, we will now describe the operation of the IPIC-QVCO. Let us assume that the tank $Q$ is high enough that only the fundamental components need to be considered. When the QVCO is operating, $M_{C2}$’s gate voltage $V_g$ has a phase of 0, and the source voltage $V_s$ has a phase of $-\pi/2$, as shown in Fig. 3(a). Since the amplitudes of $V_g$ and $V_s$ are the same, the gate-source voltage $V_{gs}$ has a phase of $-\pi/4$. Therefore, the phase of $M_{C2}$’s drain current $I_{d2}$ is also $-\pi/4$. $M_{C2}$ is turned on only when $V_{gs}$ is larger than its threshold voltage $V_t$. The conduction angle is less than $\pi$, so $M_{C2}$ works in Class-C mode.

Similarly, the phase of $M_{C1}$’s drain current $I_{d2}$ is $3\pi/4$. The current $I_{inj}$, injected into the node $I_+$ from the coupling network, is equal to $I_{d1} - I_{c2}$, as shown in Fig. 3(b). Thus, $I_{inj}$ is shifted by exactly $\pi$ compared with $I_{inj}$ or $V_{i+}$. A similar situation exists in the other three nodes $V_{Q+}$, $V_{Q-}$, and $V_{I+}$. Therefore, the in-phase coupling is realized in IPIC-QVCO. Since the coupling network does not employ any passive component, it is frequency-independent. As will be demonstrated in simulation and measurement, the parasitic capacitance has little impact on the in-phase coupling even at the mm-wave frequency.

Previous analysis assumed that the phase difference between $V_{Q+}$ and $V_{I+}$ is $\pi/2$. What happens if this phase difference is $-\pi/2$? The same analysis reveals that, in this case, $I_{inj}$ is perpendicular to $I_{inj}$, which is similar to that in the P-QVCO. Later we will prove that the second case does not exist in IPIC-QVCO. Therefore, output quadrature phases are in a known sequence that is essential for most transceivers.
B. Analysis of Oscillation Mode, Phase Error, and Phase Noise

In this subsection, we will analyze the properties of IPIC-QVCO, including oscillation mode, stability, phase error, and phase noise, based on Adler’s equation.

We start with the drain current of a diode-connected transistor in the coupling network. Assuming that its $V_i$ and $V_g$ are $V_0 \cos(\theta_1)$ and $V_0 \cos(\theta_2)$ respectively, where $\theta_1 = \omega t$, $\theta_2 = \omega t + \varphi$, $V_0$ is the oscillation amplitude, $\omega$ is the oscillation frequency, and $0 < \varphi < 2\pi$. Thus, the gate-source voltage $V_{gs}$ is

$$V_{gs} = 2V_0 \sin \left( \frac{\theta_2 - \theta_1}{2} \right) \cos \left( \frac{\theta_1 + \theta_2}{2} + \frac{\pi}{2} \right)$$

$$= 2V_0 \sin \frac{\varphi}{2} \cos \left( \omega t + \frac{\varphi}{2} + \frac{\pi}{2} \right).$$

(1)

The transistor is in saturation region when it is turned on. Due to the velocity saturation in modern transistors, as presented in Appendix A, the amplitude of its drain current at fundamental frequency is given by

$$i_d(\varphi) \approx g_{m,K} \left( V_0 \sin \left( \frac{\theta_2 - \theta_1}{2} \right) - \frac{2}{\pi} V_i \right)$$

$$= g_{m,K} \left( V_0 \sin \frac{\varphi}{2} - \frac{2}{\pi} V_i \right).$$

(2)

where $g_{m,K} = K_v n_{sat} C_{ox} W$. $K$ is the short-channel effect modeling parameter and $n_{sat}$ is the saturation velocity of the transistor. Thus, when $\varphi = \pi/2$, the amplitude of its drain current at fundamental frequency is $i_{d(\pi/2)} = g_{m,K} \left( \sqrt{2} V_0 / 2 - 2 V_i / \pi \right)$.

In this case, the amplitude of the injection current $I_{inj}$ shown in Fig. 3(b) is

$$I_{inj} = \sqrt{2} I_0 \pi/2 - g_{m,K} \left( V_0 - \frac{2 \sqrt{2}}{\pi} V_i \right).$$

(3)

According to the previous analysis, the diode-connected transistor can be modeled as a voltage-dependent transconductor as depicted in Fig. 4(a). Let us suppose that the zero-crossings of the oscillation voltage commutate the tail current $I_{t}$. In the high-$Q$ tank, only the fundamental component of the square-wave current needs to be taken into account. Thus, half of the cross-coupled regenerative pair can be modeled as the hard-limiter transconductor with an output current of $2I_0/\pi$. The whole model of IPIC-QVCO is shown in Fig. 4(b). The resonant frequency and loss of the LC tank are $\omega_0 = 1/\sqrt{LC}$ and $R$ respectively. Tank $Q$ is equal to $R C \omega_0$. We assume the four oscillation voltages in the two oscillators are $V_1 \cos(\theta_1)$, $-V_0 \cos(\theta_1)$, $V_0 \cos(\theta_2)$ and $-V_0 \cos(\theta_2)$. Therefore, according to (1) and (2), we obtain the drain currents of diode-connected transistors in the coupling network:

$I_{d1} = i_d(\theta_2 - \theta_1) \cos((\theta_1 + \theta_2)/2 + \pi/2)$,

$I_{d2} = i_d(\theta_1 - \theta_2 + \pi) \cos((\theta_1 + \theta_2)/2)$,

$I_{d3} = i_d(\theta_2 - \theta_1) \cos((\theta_1 + \theta_2)/2 - \pi/2)$,

and $I_{d4} = i_d(\theta_1 - \theta_2 + \pi) \cos((\theta_1 + \theta_2)/2 + \pi)$.

The IPIC-QVCO can be treated as two strongly coupled oscillators. Thus, applying these expressions to the generalized Adler’s equation in [16] leads to the differential equations (4) and (5) shown at the bottom of the page. We will mainly use these two differential equations to analyze the IPIC-QVCO.

$$\frac{d\theta_1}{dt} = \omega_0 + \omega_0 \frac{i_d(\theta_2 - \theta_1) \sin \left( \frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2} \right) - i_d(\theta_1 - \theta_2 + \pi) \sin \left( \frac{\theta_2 - \theta_1}{2} \right)}{2Q} - \frac{i_d(\theta_1 - \theta_2 + \pi) \cos \left( \frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2} \right)}{2} - i_d(\theta_1 - \theta_2 + \pi) \cos \left( \frac{\theta_2 - \theta_1}{2} \right)$$

(4)

$$\frac{d\theta_2}{dt} = -\omega_0 + \omega_0 \frac{-i_d(\theta_2 - \theta_1) \sin \left( \frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2} \right) + i_d(\theta_1 - \theta_2 + \pi) \sin \left( \frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2} \right) + i_d(\theta_1 - \theta_2 + \pi) \sin \left( \frac{\theta_2 - \theta_1}{2} \right)}{2Q} - \frac{i_d(\theta_1 - \theta_2 + \pi) \cos \left( \frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2} \right)}{2} + i_d(\theta_1 - \theta_2 + \pi) \cos \left( \frac{\theta_2 - \theta_1}{2} \right)$$

(5)
1) Oscillation Mode and Stability: Let us suppose the two oscillators are stable and oscillate at a common frequency \( \omega_{osc} \). Substituting \( \theta_1 = \omega_{osc} t + \phi \) and \( \theta_2 = \omega_{osc} t + \varphi \) into (4) and (5), the solutions of \( \varphi \) are \( \varphi_1 = \pi/2 \); see equation (6) at the bottom of the page, where \( m \) is the coupling strength and defined as

\[
m = \frac{i_{inj}}{I_{osc}} = \frac{i_{inj}}{I_{c}}.
\]

From the analysis of the previous subsection, we know that \( i_{inj} \) should be less than \( 2I_0/\pi \), that is \( 0 < m < 1 \). The second and third solutions are non-quadrature. The first solution indicates that the IPIC-QVCO has a phase difference of \( \pi/2 \) between the two oscillators. Substituting \( \varphi_2 = \pi/2 \) into (4) and (5) gives \( d\theta_1/dt = d\theta_2/dt = \omega_{osc} = \omega_0 \). The result is obvious: the total injection current from the coupling network \( i_{inj} \) is in phase with the oscillating current \( I_{osc} \). So there is no additional phase-shift in the tank. The oscillator operates at the resonant frequency of the \( LC \) tank as shown in Fig. 4(c). That is, the IPIC-QVCO is in-phase injection-coupled.

Perturbation analysis can be used to check the stability of this solution. A stable system should correct the perturbation by itself. We assume that the phases of the two oscillators have some small change due to perturbation: \( \theta_1 = \omega_0 t + \hat{\theta}_1 \) and \( \theta_2 = \omega_0 t + \pi/2 + \hat{\theta}_2 \), where \( |\hat{\theta}_1|, |\hat{\theta}_2| \ll 1 \). Substituting these expressions into (4) and (5) and simplifying the results, we get

\[
\frac{d(\hat{\theta}_1 - \hat{\theta}_2)}{dt} = -\frac{\sqrt{2g_{mK}V_i\omega_0}}{2QI_0(1-m)}(\hat{\theta}_1 - \hat{\theta}_2) = -\frac{1}{\tau}(\hat{\theta}_1 - \hat{\theta}_2)
\]

where \( \tau = \sqrt{2QI_0(1-m)}/(g_{mK}V_i) \) is the damping time-constant of the system. The larger coupling strength \( m \) leads to smaller \( \tau \) and a faster system in suppressing the disturbance. Since \( \tau > 0 \), any perturbation in the phase of the output voltage will decay, which means that this mode is unconditionally stable.

We can also apply perturbation analysis to check the stability of solutions \( \varphi_2,3 \). However, due to the complexity of the expressions, little information can be obtained from the expressions directly. We have varied the parameters within the range of all practical values for 60 GHz QVCO, and the quantitative analysis shows that the two solutions are unstable. In addition, these two solutions have not been observed in our simulation.

2) Phase Error due to Mismatches: In practical implementation, there are device mismatches in QVCOs because of the asymmetric layout or the process variation, which leads to phase error. The mismatches may exist in the \( LC \) tank resonant frequency, tank quality factor, coupling network, and tail current. We suppose all the mismatches are in the second oscillator: oscillation frequency \( \omega_{osc} = \omega_0 + \Delta \omega_0 \), tank quality factor \( Q_2 = Q + \Delta Q \), dimension of transistors in the coupling network \( W_{C2} = W_{C4} = W + \Delta W \), and tail current \( I_{02} = I_0 + \Delta I_0 \), and tail current \( I_{02} = I_0 + \Delta I_0 \), which results in the phase error represented by \( \Delta \varphi \). Let us assume the phase error is in the second oscillator, so its phase is \( \theta_2 = \theta_1 + \pi/2 - \Delta \varphi \). Substituting all these expressions into (4) and (5) and simplifying the results, we obtain

\[
\Delta \varphi = \sqrt{2QI_0(1-m)}\Delta \omega_0 + \frac{1-\sqrt{2\pi V_0}}{4V_i}\frac{\Delta W}{W} + \frac{\Delta V}{V_i} + \frac{\Delta V}{V_i}
\]

where \( \tau = \tau(1-m)/g_{mK}V_i \) is the damping time-constant of the system. The larger coupling strength \( m \) leads to smaller \( \tau \) and a faster system in suppressing the disturbance. Since \( \tau > 0 \), any perturbation in the phase of the output voltage will decay, which means that this mode is unconditionally stable.

Similar to the P-QVCO, if the coupling strength \( m \) increases or tank \( Q \) decreases, the phase error of IPIC-QVCO due to \( \varphi_2 \) mismatch decreases. Interestingly, \( \tau \) also represents the suppression of phase error due to \( \omega_0 \) mismatch because a small \( \tau \) results in a small phase error. Fig. 5 compares the real transistor simulated and calculated phase errors due to mismatches in the coupling network and \( \omega_0 \). The oscillation frequency is set to 60 GHz, with a tank \( Q \) of 6, tail current of 5 mA, and coupling strength of 0.2. The theoretical results show good agreement with the simulation results.

It is noteworthy that, as implied by (9), the quadrature accuracy is not affected by mismatches of \( Q \) and \( I_0 \), but by the mismatch in the coupling network. This seemingly contradictory phenomenon can be explained with voltage and current phasor diagrams. Suppose the IPIC-QVCO has quadrature outputs in the initial state with no mismatch. Mismatches of \( Q \) and \( I_0 \) will cause the amplitude of output voltages in the second oscillator to change as depicted in Fig. 6(a). Although \( V_{osc,i} \) and \( I_{inj,i} \) are changed, \( I_{inj,i} \) is still in phase with the output voltage and \( I_{osc,i} \). Therefore, the QVCO remains locked to \( \omega_0 \) with quadrature output phases. On the other hand, \( \Delta V \) in the coupling network will change \( I_{o2} \) and

\[
\varphi_{2,3} = 2 \arctan \left( \frac{1}{4g_{mK}V_i} \left( \pi g_{mK}V_i - 2I_0 \pm 2 \sqrt{I_0(1-m)}(\pi g_{mK}V_0 - I_0(1+m)) \right) \right)
\]
Fig. 6. Voltage and current phasor diagrams due to (a) $Q$, $I_c$, and (b) coupling network mismatches.

$I_{d4}$, instead of $V_{gs,i}$, as shown in Fig. 6(b). Thus, $I_{nj1}$ has a phase-shift with $I_{osc,i}$. The different phase-shifts in the two oscillators will cause their output phases to depart from quadrature, and thus phase error appears. Fortunately, since the coupling network is simple and symmetric, the mismatch caused by the layout is small. The phase error is less than $1\degree$ within a 5% mismatch in the coupling network as depicted in Fig. 5.

3) Phase Noise: Phase noise can be analyzed as weak injection by using Alder’s equation. We treat white noise in each device as individual weak injection current into the two oscillators. The injection currents directly or indirectly lead to phase noise. By following the steps in [16], the phase noise caused by the white noise in the tank, cross-coupled pair, and coupling network can be derived from (4) and (5):

$$L(\omega_m) = \frac{k_B T \omega_0 (1 + \gamma(1 + m)^2)}{2 Q C V_o (1 - m)^2 \omega_n^2}$$

where $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, and $\gamma$ is the MOS channel noise factor. The effective output voltage is $V_{eff} = V_c (1 - m)$. The factor $m$ represents the ratio of current flow into the coupling network. This is similar to the P-QVCO if we merge the tail current source in the cross-coupled pair and the coupling network, because a portion of $I_0$ is consumed by the coupling network. In contrast to the phase error, the phase noise of IPIC-QVCO due to white noise increases with coupling strength and decreases with tank $Q$. Therefore, there are trade-offs in coupling strength and tank $Q$ when considering both phase error and phase noise in IPIC-QVCO design. Fig. 7 compares the simulated phase noise and calculated phase noise using (10), and the difference is less than 1.5 dB.

Flicker noise in the cross-coupled pair of a differential $LC$ oscillator contributes to negligible phase noise since it is sampled at twice the oscillation frequency [25]. However, flicker noise in the coupling network of P-QVCO introduces significant phase noise. This is because in the real circuit, the oscillation frequency of P-QVCO depends on the transconductance of the coupling network $G_{u,C}$. The flicker noise slowly modulates $G_{u,C}$ and is up-converted into the close-in $1/f^3$ phase noise [26]. In addition, the noise current injects at the zero-crossing of the output voltage, exacerbating the flicker noise up-conversion. In contrast to the P-QVCO, the oscillation frequency of the IPIC-QVCO is $\omega_0$ which is independent of the transistors, and the coupling is in phase. Thus, the influence of flicker noise in the coupling network of IPIC-QVCO is not so critical. This can be verified through the impulse sensitivity function (ISF) simulation [27]. NMF is the normalized instantaneous drain current in one oscillation cycle. Effective ISF is the product of ISF and NMF. It is obvious from the simulation that, compared with P-QVCO, IPIC-QVCO has much smaller DC value and root mean square value of the effective ISF, resulting in less flicker noise up-conversion and lower phase noise.

Flicker noise in tail current source is another serious issue in P-QVCO. Analyzing IPIC-QVCO by using (4) and (5) gives that flicker noise in tail current source does not contribute to phase noise directly. The flicker noise varies the amplitude of the output voltage, and is converted into the close-in $1/f^3$ phase noise through a varactor. The difference of flicker noise up-conversion between P-QVCO and IPIC-QVCO can be demonstrated in simulation. The tail current sources in Fig. 2 are implemented with NMOS current mirrors, and the same conditions in Fig. 5 are adopted. Simulation results depict that, the phase noise of IPIC-QVCO due to flicker noise in tail current source is at least 3 dB lower than that of P-QVCO. Therefore, IPIC-QVCO also desensitizes flicker noise in tail current source up-conversion.

C. 60 GHz IPIC-QVCO Design

Fig. 8 shows the full schematic of 60 GHz IPIC-QVCO. The coupling network without the gate bias voltage $V_{gb}$ (i.e., formed by direct diode-connected transistors) is used in PLL, while the coupling network with $V_{gb}$ is used in a standalone QVCO to explore the characteristics of the in-phase injection coupling.

A 3-bit binary-weight switch-capacitor bank is used for discrete tuning. The resistor-biased switch contributes to less noise than other conventional switches [28]. Metal-oxide-metal (MOM) capacitors are used for their small capacitance and convenient layout. A small p-type varactor is used for continuous tuning. $I_0$ represents the digitally controlled variable resistor in order to reduce flicker noise. The DC voltage of the oscillation nodes is set to about half of the supply voltage $V_{DD}$.
to fully utilize the tuning characteristic of the varactor. The eight overlapped bands can cover the four required frequency spots in IEEE 802.15.3c with low VCO gain ($K_{\text{VCO}}$).

The passive devices such as inductors and transmission lines are all custom designed. Since the parasitics of interconnects and devices play important roles in the mm-wave circuit design, we use an electromagnetic (EM) simulator to obtain their S-parameters. The S-parameters files are then sent back to Cadence SpectreRF for circuit simulation with active devices. Because the $f_{\text{MAX}}$ of 65 nm transistors is sufficient high for 60 GHz application, the model described in the previous subsection is valid as long as the tank or S-parameters files take the parasitics of interconnects and devices into account.

As mentioned previously, there is a trade-off between phase noise and phase error in terms of the coupling strength $m$. We can choose a proper $m$ and power to meet the phase noise and phase error requirements simultaneously. However, to get a particular $m$ is tedious for the mm-wave circuit design, because it is difficult to distinguish the currents flowing into the transistors and their parasitics. A more efficient method for mm-wave circuit design is through simulation iterations. We define the coupling factor $\alpha$ as the ratio of the transistor’s width in the coupling network to the transistor’s width in the cross-coupled regenerative pair. Note that in IPIC-QVCO, $m$ is determined by the coupling factor $\alpha$ and the bias voltage $V_b$. Simulations are carried out to find the optimum values of $\alpha$ and $V_b$. We choose $f_c = 60$ GHz, $M_R = 20 \mu$m/$0.06 \mu$m, $I_t = 60 \mu$A, $Q_I = 15$, $I_0 = 5$ mA. Fig. 9 shows the simulated phase noise and phase error by varying $\alpha$ and $V_b$. We note that the phase error is small and does not change much if $\alpha > 0.5$ and $V_b > 0.3$ V. So the coupling network without $V_b$, which is used in our QPLL, can achieve good performance. In our design, to ensure the start-up and the wide tuning range under the process and temperature variation, a small coupling network is chosen. $W_H$ is set to 20 $\mu$m, and $\alpha$ is chosen as 1/3.

We also compare IPIC-QVCO with other conventional QVCOs: P-QVCO, bottom series QVCO [29], superharmonic-coupled QVCO [30], and magnetically-coupled QVCO [17]. Unless otherwise stated, all the conditions are the same. The simulated performances are summarized in Table I. Compared with other conventional QVCOs, the IPIC-QVCO has large output amplitude, good phase noise, and good phase error. Moreover, the IPIC-QVCO exhibits good performance at multi-GHz frequencies in our simulation.
III. DIVIDER CHAIN AND CHARGE PUMP DESIGN

A. Low Power Inductor-Less Divider Chain

Designing frequency dividers is challenging in mm-wave PLL since they may consume substantial power. Large area is another issue due to the use of inductors. In this work, the inductor-less DCML divider, ILFD, and TSPC divider are implemented in cascade. By using these divider topologies, the low power and small area can be achieved simultaneously. We will describe them separately.

Fig. 10(a) depicts the schematic of the modified DCML divide-by-4 frequency divider. Compared with a traditional CML divider, the DCML divider uses the parasitic capacitor in differential amplifier pair, instead of a static cross-coupled latch, to store the data [21]. By removing the cross-coupled pairs, the maximum operation frequency of the divider is increased, making it suitable for mm-wave frequency. To further improve its performance, two methods have been adopted. Firstly, low threshold voltage (low-Vt) devices are used to increase the maximum operation frequency for their higher S. Secondly, we merge the switches of the same input clock of the DCML divider in [21], i.e., node $X_\text{A}$ and node $X_\text{B}$ are connected together. By connecting $X_\text{A}$ and $X_\text{B}$, we now present a balanced and high conductance point at the input frequency. Therefore, the injection currents of the modified DCML divider are larger than that of the conventional DCML divider, as shown in Fig. 10(c). From the point of view of injection locking, the locked bandwidth of the modified DCML divider is enlarged. In order to balance the output loadings, all the eight-phase outputs of the DCML divider serve as the inputs of the next divider. Fig. 10(b) shows its post-layout simulation results with different bias voltages $V_{\text{bp}}$. With about 300 mV peak-to-peak input voltage, the divider works from 35 GHz to 77 GHz, with at least 3 GHz bandwidth in each sub-band. Thus, two sub-bands can cover the four frequency spots of IEEE 802.15.3c. The simulated power consumption is about 9.0 mW at 60 GHz frequency, at a 1.2 V supply.

Fig. 11(a) depicts the schematic of the injection-locked divide-by-4 frequency divider. Its eight-phase inputs are from the outputs of the DCML divider. Each two adjacent phase inputs are added through transistors to generate four injection currents. The four injection currents are in quadrature with enhanced amplitude as shown in Fig. 11(b). The multiphase injection with proper sequence can improve the locking range of the divide-by-4 ILFD divider.
Fig. 11. (a) Schematic, (b) phasor of injection current, and (c) simulated locking range of the injection-locked divide-by-4 divider.

[31]. Fig. 11(c) shows its post-layout simulation results with different bias voltages $V_{by2}$. With about 300 mV peak-to-peak input voltage, the divider works from 8 GHz to 28 GHz. The locking range of each sub-band is large enough to cover about 5 GHz input range. The simulated power consumption is less than 3.2 mW with a 1.2 V supply.

The multi-modulus divider consists of four divide-by-2/3 TSPC divider cells and one control circuit. It can realize the four-division modulus (27, 28, 29, and 30) with low power consumption. The output of the multi-modulus divider is taken from the first divide-by-2/3 divider to reduce the phase noise, because it is retimed by the high frequency input. The simulated power consumption is about 0.7 mW.

B. Low Spur Charge Pump

The programmable, self-correcting low spur CP, shown in Fig. 12(a), is modified from [32]. The voltage-to-current (VI) converter, which includes a rail-to-rail amplifier, senses the voltage difference between $V_1$ and $V_2$, and corrects the mismatch between charge and discharge currents. Thus, the static phase offset is minimized and the effective tuning range is maximized. However, there are two problems in [32]: clock feedthrough and charge injection in the switches. In our proposed charge pump, two measures are taken to avoid these two problems and further reduce spurious level. First, the UP/DN switches are moved to the source of current source transistors to eliminate the clock feedthrough and charge injection. Second, the VCO control voltage $V_{ctrl}$ is connected to $V_1$, instead of $V_2$. So $V_1$ can be regarded as $V_2$ after a unity-gain amplifier. The benefit is that the ripple in $V_2$ caused by the reference clock can be filtered by this follower as long as its bandwidth $f_{amp}$ is less than the reference frequency $f_{ref}$. It also isolates the switches and $V_1$, so the clock has negligible effect on the output. On the other hand, $f_{amp}$ is designed to be significantly larger than the PLL loop bandwidth $f_{PLLBW}$, to minimize the effect on the system loop characteristics and stability. In this design, $f_{PLLBW}$ can be programmed from 0.5 to 2 MHz, and $f_{amp}$ and $f_{ref}$ are about 40 and 135 MHz, respectively. Fig. 12(b) depicts the simulated waveforms of $V_{ctrl}$ when it is connected to $V_1$ and $V_2$ respectively. As expected, the amplifier does not interfere with the locking process. The ripple of $V_{ctrl}$ connected to $V_1$ is much smaller, and is reduced by about 10 times compared with that connected to $V_2$. We also performed a transient simulation to observe the reference spur levels with non-idealities: 10% charge/discharge current mismatch and 1 nA leakage current in the LPF as shown in Fig. 12(c). When $V_{ctrl}$ is connected to $V_1$, the reference spur is consistently reduced by about 10 dB compared with when $V_{ctrl}$ is connected to $V_2$. The simulated power consumption of this charge pump is about 0.3 mW.

IV. EXPERIMENTAL RESULTS

A 60 GHz standalone IPIC-QVCO and a 60 GHz PLL are implemented in GLOBALFOUNDRIES standard 65 nm low power CMOS technology. Fig. 13 shows the die micrograph of the standalone QVCO and the complete PLL, which occupy 0.26 $\times$ 0.15 mm$^2$ and 0.32 $\times$ 0.60 mm$^2$, respectively.

The standalone IPIC-QVCO consumes 11.4 mW (not including output buffers) from a 1.2 V supply. The measured VCO tuning curves are shown in Fig. 14. The eight bands of the QVCO cover a frequency range of 57.88 to 68.33 GHz, i.e., 16.6% around the center frequency, with a tuning sensitivity less than 2 GHz/V. As depicted in Fig. 15, the measured QVCO phase noises for a 62.66 GHz carrier are -94.2 and -115.0 dBc/Hz at 1 and 10 MHz offset, respectively. The corner frequency between the $1/f^2$ and $1/f^4$ region is less
than 2 MHz, demonstrating a low flicker noise up-conversion. Note that the corner frequency can be further reduced if the size of the diode-connected transistors in the coupling network is larger. We also measured the phase noise performance across the tuning range from six samples. The phase noise is between $-92$ and $-95$ dBc/Hz at 1 MHz offset. The Figure of Merit (FOM) and FOM$_T$ are $-178.1$ $-179.7$ and $-182.5$ $-184.1$ dBc/Hz at 1 MHz offset, respectively. The phase and amplitude errors are measured by down-converting the quadrature signals to about 250 MHz. Fig. 17 shows that the phase error is less than 0.7° and the amplitude error is less than 0.9 dB across 6 samples for $V_i$. To verify the characteristics of the in-phase coupling, we measure the IPIC-QVCO by varying the bias voltage $V_b$, as depicted in Fig. 18. Measurement results show that the frequency is almost constant when $V_b$ increases, indicating the coupling is in phase. The phase noise increases and the phase error decreases while the coupling strength becomes stronger, which coincides with the analysis results. Table II shows the summarized measurement results and a comparison with other state-of-the-art 60 GHz CMOS QVCOs. The proposed IPIC-QVCO has good phase noise and small phase error, and consumes the least power.

The PLL consumes 24.6 mW (not including open-drain output buffers) from a 1.2 V supply, of which, about 11.4, 12.7, and 0.5 mW are consumed by QVCO, divider chain and other blocks, respectively. The operation range of the PLL is from 57.9 to 68.3 GHz. When the reference input $f_{ref} = 135$ MHz, the PLL can be locked to the four frequencies defined by the IEEE 802.15.3c standard: 58.32, 60.48, 62.64, and 64.80 GHz. As shown in Fig. 19, PLL phase noise is $-91.0$ dBc/Hz at 1 MHz offset from a 62.64 GHz carrier. Phase noise contributors are also plotted in Fig. 19 through a combination

![Fig. 12. (a) Schematic and (b) simulated output voltages of the proposed charge pump. [Please include a subcaption for part (c).]](image)

![Fig. 13. Die photographs of the standalone IPIC-QVCO and the complete PLL.](image)
TABLE II
COMPARISON OF STATE-OF-THE-ART 60 GHZ CMOS QVCOS

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Tech.</th>
<th>Supply Voltage (V)</th>
<th>Freq. Tuning Range (GHz) (FTR%)</th>
<th>Phase Noise @1MHz (dBC/Hz)</th>
<th>FOM(^{(a)}) (dBC/Hz)</th>
<th>FOM(^{(b)}) (dBC/Hz)</th>
<th>Phase Error</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[13]</td>
<td>45 nm</td>
<td>1.1</td>
<td>57 ~ 66 (14.6%)</td>
<td>-75(^{(a)})</td>
<td>-156.3</td>
<td>-159.6</td>
<td>n.a.</td>
<td>28</td>
</tr>
<tr>
<td>[17]</td>
<td>65 nm</td>
<td>1.0</td>
<td>56.0 ~ 60.4 (7.6%)</td>
<td>-95 ~ -97</td>
<td>-177 ~ -179</td>
<td>-174.6 ~ -176.6</td>
<td>&lt; 1.5°</td>
<td>22</td>
</tr>
<tr>
<td>[35]</td>
<td>65 nm</td>
<td>1.2</td>
<td>57.5 ~ 63.1 (9.3%)</td>
<td>-95.3</td>
<td>-174.9</td>
<td>-174.3</td>
<td>n.a.</td>
<td>36</td>
</tr>
<tr>
<td>[36]</td>
<td>65 nm</td>
<td>1.2</td>
<td>54.0 ~ 61.0 (24.3%)</td>
<td>-90.0 ~ -94.0</td>
<td>-173 ~ -176</td>
<td>-181 ~ -184</td>
<td>n.a.</td>
<td>15.6 ~ 30.0</td>
</tr>
<tr>
<td>This Work</td>
<td>65 nm</td>
<td>1.2</td>
<td>57.88 ~ 68.33 (16.6%)</td>
<td>-92 ~ -95</td>
<td>-178.1 ~ 179.7</td>
<td>-182.5 ~ 184.1</td>
<td>&lt; 0.7°</td>
<td>11.4</td>
</tr>
</tbody>
</table>

\(^{(a)}\) FOM = L(Δf) + 20\log(Δf/f₀) + 10\log(Power/1mW).

\(^{(b)}\) FOM\(_T\) = L(Δf) + 20\log(Δf/f₀) (FTR/10) + 10\log(Power/1mW).

\(^{(c)}\) PLL phase noise.

Fig. 14. Measured tuning range of the IPIC-QVCO.

Fig. 15. Measured phase noise of the IPIC-QVCO.

The measured QVCO and PLL performance are summarized and compared with state-of-the-art works in Table III. Our PLL has a simple structure and can achieve good performance with ultra-low power consumption.

V. CONCLUSION

A low power fully integrated 60 GHz quadrature PLL is reported. Through a particular symmetrical coupling network, the in-phase coupling is realized in the proposed IPIC-QVCO, which reduces both phase noise and phase error. Implemented in standard 65 nm low power CMOS technology, the PLL operates from 57.9 to 68.3 GHz with 24.6 mW power consumption. PLL phase noise is from -89.8 to -91.0 dBc/Hz at 1 MHz offset across the frequency band. The reference spur is less than -54.5 dBc. This work supports IEEE 802.15.3c and other compatible 60 GHz standards. To the authors’ knowledge, our work has the least power consumption in reported quadrature frequency synthesizers for IEEE 802.15.3c and other compatible 60 GHz standards. The IPIC-QVCO shows great potential for high performance QVCOS in both low frequency and mm-wave applications.

APPENDIX

This Appendix shows the derivation of the drain current amplitude of a diode-connected transistor at fundamental frequency. Fig. 22 shows the gate-source voltage \(V_{gs}\) and the...
Table III

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Tech.</th>
<th>Supply Voltage (V)</th>
<th>Ref. Freq. (MHz)</th>
<th>Freq. Tuning Range (GHz) (FTR%)</th>
<th>Phase Noise @ 1MHz Offset (dBc/Hz)</th>
<th>Ref. Spur (dBc)</th>
<th>Topology</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>90 nm</td>
<td>0.7 / 1.2</td>
<td>117</td>
<td>59.6 ~ 64.0 (7.1%)</td>
<td>-72.5</td>
<td>-23</td>
<td>30 GHz PLL + 60 GHz Hybrid</td>
<td>76.3</td>
</tr>
<tr>
<td>[7]</td>
<td>65 nm</td>
<td>1.0 / 1.2</td>
<td>36</td>
<td>54 ~ 61 (12.2%)</td>
<td>-94.2</td>
<td>n.a</td>
<td>20 GHz PLL + 60 GHz QVCO</td>
<td>80.9</td>
</tr>
<tr>
<td>[9]</td>
<td>40 nm</td>
<td>1.1</td>
<td>20000</td>
<td>55 ~ 66 (18.2%)</td>
<td>&lt; -96</td>
<td>n.a</td>
<td>60 GHz QVCO</td>
<td>112</td>
</tr>
<tr>
<td>[13]</td>
<td>45 nm</td>
<td>1.1</td>
<td>100</td>
<td>57 ~ 66 (14.6%)</td>
<td>-75</td>
<td>-42</td>
<td>60 GHz QPLL</td>
<td>78</td>
</tr>
<tr>
<td>[37]</td>
<td>40 nm</td>
<td>1.1</td>
<td>n.a.</td>
<td>63 ~ 70 (10.5%)</td>
<td>-85</td>
<td>&lt; -40</td>
<td>60 GHz QPLL</td>
<td>66</td>
</tr>
<tr>
<td>This Work</td>
<td>65 nm</td>
<td>1.2</td>
<td>135</td>
<td>57.9 ~ 68.3 (16.5%)</td>
<td>-89.8 ~ -91.5</td>
<td>-54.5</td>
<td>60 GHz QPLL</td>
<td>24.6</td>
</tr>
</tbody>
</table>

(a) QVCO = Quadrature injection-locked oscillator.

where \(2 \arcsin\left(\frac{V_i}{(2V_0)}\right) < \varphi < 2\pi - 2\arcsin\left(\frac{V_i}{(2V_0)}\right)\), to ensure the transistor is turned on and works in saturation region.

In a modern transistor, when \(V_{ds}\) is larger than saturation drain voltage \(V_{ds,sat}\), the carrier drift velocity saturates. In a diode-connected transistor, the saturation region meets this condition because usually \(V_{ds,sat} < V_i\). Therefore, the drain current is given by [33]

\[
I_d = g_{mK}(V_{gs} - V_i) = g_{mK} \left(2V_0 \sin \frac{\varphi}{2} \cos \omega t - V_i\right) \quad (13)
\]

where \(g_{mK} = K_{\text{sat}}C_{ox}W\), \(K\) is the short-channel effect modeling parameter and \(v_{sat}\) is the saturation velocity of a transistor.

Since we assume the tank \(Q\) is high enough, only the fundamental current is considered. The fundamental term of \(I_d\) in the Fourier series is computed as follows:

\[
i_d = \frac{\omega}{\pi} \int_{\varphi/\omega}^{\varphi/\omega} g_{mK} \left(2V_0 \sin \frac{\varphi}{2} \cos \omega t - V_i\right) \cos \omega t dt = \frac{g_{mK}}{\pi} \left(2V_0 \sin \frac{\varphi}{2} \left(2\Phi + \sin 2\Phi\right) - 2V_i \sin \Phi\right) \quad (14)
\]
Fig. 19. Measured and simulated phase noise of the PLL.

Substituting (12) and using the series of \( \arccos(x) = \pi/2 - x - x^3/6 + \cdots \) for \( 2 \arcsin \left( \frac{V_i}{2V_o} \right) < \varphi < 2\pi - 2\arcsin \left( \frac{V_i}{2V_o} \right) \), we can simplify (14) as

\[
i_c(\varphi) \approx 2mK \left( \frac{V_o}{2\pi} \right) \sin \frac{\varphi}{2},
\]

(15)

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REFERENCES

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A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer With In-Phase Injection-Coupled QVCO in 65 nm CMOS Technology

Xiang Yi, Member, IEEE, Chirn Chye Boon, Senior Member, IEEE, Hang Liu, Jia Fu Lin, Student Member, IEEE, and Wei Meng Lim

Abstract—A fully integrated 60 GHz frequency synthesizer with an in-phase injection-coupled quadrature voltage-controlled oscillator (IPIC-QVCO) is proposed. Through a particular symmetrical coupling network formed by diode-connected transistors, the in-phase coupling is realized in the IPIC-QVCO, which reduces both phase noise and phase error. A compact inductor-less divider chain is designed to reduce power consumption. A self-correcting low spur charge pump is employed to reduce reference spur. A standalone 60 GHz IPIC-QVCO and a fully integrated PLL are implemented in standard 65 nm low power CMOS technology. The measurement results show that the QVCO covers a frequency range from 57.88 to 68.33 GHz while consuming 11.4 mW power from a 1.2 V supply. The phase noise of the QVCO is –92 ~ –95 dBc/Hz at 1 MHz offset. The FOM and FOMT of the QVCO are –178.1 ~ –179.7 and –182.5 ~ –184.1 dBc/Hz respectively. The tuning range of the frequency synthesizer is from 57.9 to 68.3 GHz, and the power consumption is 24.6 mW. The phase noise of the frequency synthesizer is –89.8 ~ –91.5 dBc/Hz at 1 MHz offset across the frequency band.

Index Terms—CMOS, frequency synthesizer, in-phase injection-coupled (IPIC), low phase error, low phase noise, low power, millimeter-wave, PLL, quadrature voltage-controlled oscillator (QVCO), 60 GHz.

I. INTRODUCTION

NEXT-GENERATION short range high data rate wireless communication in the unlicensed 60 GHz frequency band was intensively investigated in the last decade. As defined in the 60 GHz standards, such as IEEE 802.15.3c, IEEE 802.11ad, WiGig, WirelessHD, and ECMA-387 [1]–[5], the total 9 GHz (57–66 GHz) bandwidth is divided into four 2.16 GHz channels. To achieve a higher data rate, complex modulations such as 16-QAM must be adopted, which increases the requirements of local oscillator’s (LO’s) phase noise and phase error. In recent years, it has already been demonstrated that advanced CMOS technology has the capability of realizing millimeter-wave (mm-wave) integrated circuits. CMOS implementation can reduce cost and improve yield, since RF front-end can be integrated with analog and digital baseband circuits.

Direct-conversion architecture is popular for 60 GHz transceivers because of its simple structure and fewer components [6]–[12]. Phase locked-loop (PLL) is an important block in a transceiver. Design of the wide range, low phase noise, low phase error and low power CMOS PLL for the 60 GHz direct-conversion transceiver is challenging, due to trade-offs between tuning range, phase noise, phase error, and power consumption. There are many methods for generating mm-wave quadrature LO signals, but they suffer from many problems. 1) The most common method is through a conventional mm-wave parallel quadrature voltage-controlled oscillator (P-QVCO), but its phase noise is poor [13]. 2) The method of using a divide-by-2 divider after a VCO with double LO frequency prevails in multi-GHz applications, but it is difficult to design a VCO and a divider at very high frequency. Moreover, the power consumption of this method is high. 3) If passive components such as an RC polyphase filter or quadrature hybrid coupler are used to produce quadrature signals, we usually need buffers to compensate their loss, so the power consumption is also high [6]. 4) Using an injection-locked multiplier is a good choice [14], but the disadvantages are limited locking range and intrinsic phase error due to the imbalance of the structure, or quadrature inputs are needed to overcome these drawbacks [9].

In this work, we present a wide range, low phase noise, and low power 60 GHz quadrature PLL [15]. The simplified block diagram of the proposed PLL is shown in Fig. 1. It is an integer-N third-order charge-pump PLL with a 135 MHz reference input. The 60 GHz in-phase injection-coupled (IPIC) QVCO is proposed to reduce phase noise and phase error. Its operation frequency can cover the four required frequency spots in IEEE 802.15.3c and other compatible 60 GHz standards. The low power inductor-less frequency divider chain consists of a modified divide-by-4 dynamic current-mode logic (DCML) divider, a divide-by-4 multi-phase injection-locked frequency divider (ILFD), and a multi-modulus true-single-phase-clock (TSPC) divider. The low spur self-correcting charge pump is employed to reduce the reference spur. A standalone 60 GHz IPIC-QVCO and a fully integrated 60 GHz PLL are implemented in standard 65 nm low power CMOS technology to demonstrate our ideas. Measurement results show that the proposed IPIC-QVCO and quadrature PLL can achieve good performance with low power consumption.
The paper is organized as follows. Section II discusses the proposed IPIC-QVCO, including architecture, analysis, and circuit design. Section III describes the frequency divider chain and charge pump design. Experimental results are provided in Section IV and conclusions are drawn in Section V.

II. IN-PHASE INJECTION-COUPLED QVCO

A. Proposed In-Phase Injection-Coupled QVCO

In general, the QVCO consists of two identical oscillators pulling each other, through coupling networks, to lock at a common frequency with quadrature phase. It is well known that in QVCO, the in-phase coupling can reduce both phase noise and phase error [16]. Many phase shifting techniques were presented to realize the in-phase coupling [16]–[21]. But their coupling networks are either $RC$-based or $LC$-based phase shifters, which are both frequency-dependent.

The in-phase coupling is realized in the proposed IPIC-QVCO by using the frequency-independent network, instead of the frequency-dependent phase shifter. In fact, the most neglected thing is that, quadrature signals always exist in a QVCO inherently. Therefore, intuitively, in-phase coupling can be realized through a particular symmetrical coupling network. Similar concepts have already been demonstrated in multiphase injection ILFDs [22]–[24]. We will prove that this concept also works in our QVCO. The schematic of the proposed QVCO is shown in Fig. 2. The two identical differential $LC$ cross-coupled VCOs are coupled through a symmetrical coupling network. In the coupling network, each diode-connected transistor connects two oscillation nodes with $\pi/2$ phase difference, e.g., transistor $M_{C1}$ connects node $Q+$ and node $I+$. So the four diode-connected transistors form a symmetrical ring. As will be analyzed later, this configuration can generate in-phase injection current with the tank current.

To understand the basic concept of the in-phase coupling, we will now describe the operation of the IPIC-QVCO. Let us assume that the tank $Q$ is high enough that only the fundamental components need to be considered. When the QVCO is operating, $M_{C2}$’s gate voltage $V_g$ has a phase of 0, and the source voltage $V_s$ has a phase of $-\pi/2$, as shown in Fig. 3(a). Since the amplitudes of $V_g$ and $V_s$ are the same, the gate-source voltage $V_{gs}$ has a phase of $\pi/4$. Therefore, the phase of $M_{C2}$’s drain current $I_{d2}$ is also $\pi/4$. $M_{C2}$ is turned on only when $V_{gs}$ is larger than its threshold voltage $V_t$. The conduction angle is less than $\pi$, so $M_{C2}$ works in Class-C mode.

Similarly, the phase of $M_{C1}$’s drain current $I_{d2}$ is $3\pi/4$. The current $I_{inj}$, injected into the node $I+$ from the coupling network, is equal to $I_{d1} - I_{d2}$, as shown in Fig. 3(b). Thus, $I_{inj}$ is shifted by exactly $\pi$ compared with $I_{inj}$ or $V_{i+}$. A similar situation exists in the other three nodes $V_{Q+}$, $V_{Q-}$, and $V_{i-}$. Therefore, the in-phase coupling is realized in IPIC-QVCO. Since the coupling network does not employ any passive component, it is frequency-independent. As will be demonstrated in simulation and measurement, the parasitic capacitance has little impact on the in-phase coupling even at the mm-wave frequency.

Previous analysis assumed that the phase difference between $V_{Q+}$ and $V_{i+}$ is $\pi/2$. What happens if this phase difference is $-\pi/2$? The same analysis reveals that, in this case, $I_{inj}$ is perpendicular to $I_{osc}$, which is similar to that in the P-QVCO. Later we will prove that the second case does not exist in IPIC-QVCO. Therefore, output quadrature phases are in a known sequence that is essential for most transceivers.
B. Analysis of Oscillation Mode, Phase Error, and Phase Noise

In this subsection, we will analyze the properties of IPIC-QVCO, including oscillation mode, stability, phase error, and phase noise, based on Adler’s equation.

We start with the drain current of a diode-connected transistor in the coupling network. Assuming that its \(V_t\) and \(V_c\) are \(V_0 \cos(\theta_1)\) and \(V_0 \cos(\theta_2)\) respectively, where \(\theta_1 = \omega t\), \(\theta_2 = \omega t + \varphi\). \(V_0\) is the oscillation amplitude, \(\omega\) is the oscillation frequency, and \(0 < \varphi < 2\pi\). Thus, the gate-source voltage \(V_g\) is

\[
V_{g_{1,2}} = 2V_0 \sin \left(\frac{\theta_2 - \theta_1}{2}\right) \cos \left(\frac{\theta_1 + \theta_2}{2} + \frac{\pi}{2}\right)
= 2V_0 \sin \left(\frac{\varphi}{2} + \frac{\pi}{4}\right).
\]

The transistor is in saturation region when it is turned on. Due to the velocity saturation in modern transistors, as presented in Appendix A, the amplitude of its drain current at fundamental frequency is given by

\[
i_{d}(\varphi) \approx g_{mK} \left(V_0 \sin \left(\frac{\theta_2 - \theta_1}{2}\right) - \frac{2}{\pi} V_t\right)
= g_{mK} \left(V_0 \sin \left(\frac{\varphi}{2} - \frac{2}{\pi} V_t\right)\right)
\]

(2)

where \(g_{mK} = KV_{sat}C_{ox}W\), \(K\) is the short-channel effect modeling parameter and \(v_{sat}\) is the saturation velocity of the transistor. Thus, when \(\varphi = \pi/2\), the amplitude of its drain current at fundamental frequency is \(i_{d, \pi/2} = g_{mK} \left(\sqrt{2}V_0/2 - 2V_t/\pi\right)\).

In this case, the amplitude of the injection current \(i_{n, j}\) shown in Fig. 3(b) is

\[
i_{n, j} = \sqrt{2}i_{d, \pi/2} = g_{mK} \left(V_0 - \frac{2\sqrt{2}}{\pi} V_t\right).
\]

According to the previous analysis, the diode-connected transistor can be modeled as a voltage-dependent transconductor as depicted in Fig. 4(a). Let us suppose that the zero-crossings of the oscillation voltage commutate the tail current \(I_0\). In the high-\(Q\) tank, only the fundamental component of the square-wave current needs to be taken into account. Thus, half of the cross-coupled regenerative pair can be modeled as the hard-limiter transconductor with an output current of \(2I_0/\pi\). The whole model of IPIC-QVCO is shown in Fig. 4(b). The resonant frequency and loss of the LC tank are \(\omega_0 = 1/\sqrt{LC}\) and \(R\) respectively. Tank \(Q\) is equal to \(RC\omega_0\). We assume the four oscillation voltages in the two oscillators are \(V_0 \cos(\theta_1)\), \(-V_0 \cos(\theta_1)\), \(V_0 \cos(\theta_2)\) and \(-V_0 \cos(\theta_2)\). Therefore, according to (1) and (2), we obtain the drain currents of diode-connected transistors in the coupling network: \(I_{d1} = i_d(\theta_2 - \theta_1) \cos((\theta_1 + \theta_2)/2 + \pi/2)\), \(I_{d2} = i_d(\theta_2 - \theta_1) \cos((\theta_1 + \theta_2)/2)\), \(I_{d3} = i_d(\theta_2 - \theta_1) \cos((\theta_1 + \theta_2)/2 - \pi/2)\), and \(I_{d4} = i_d(\theta_1 - \theta_2 + \pi) \cos((\theta_1 + \theta_2)/2 + \pi)\).

The IPIC-QVCO can be treated as two strongly coupled oscillators. Thus, applying these expressions to the generalized Adler’s equation in [16] leads to the differential equations (4) and (5) shown at the bottom of the page. We will mainly use these two differential equations to analyze the IPIC-QVCO.

\[
\frac{d\theta_1}{dt} = \omega_0 + \frac{i_d(\theta_2 - \theta_1) \sin \left(\frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2}\right) - i_d(\theta_1 - \theta_2 + \pi) \sin \left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{2}\right)}{2Q \frac{\pi}{2} I_0 + i_d(\theta_2 - \theta_1) \cos \left(\frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2}\right) - i_d(\theta_1 - \theta_2 + \pi) \cos \left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{2}\right)}
\]

(4)

\[
\frac{d\theta_2}{dt} = \omega_0 + \frac{-i_d(\theta_2 - \theta_1) \sin \left(\frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2}\right) + i_d(\theta_1 - \theta_2 + \pi) \sin \left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{2}\right)}{2Q \frac{\pi}{2} I_0 - i_d(\theta_2 - \theta_1) \cos \left(\frac{\theta_2 - \theta_1}{2} + \frac{\pi}{2}\right) + i_d(\theta_1 - \theta_2 + \pi) \cos \left(\frac{\theta_1 - \theta_2}{2} + \frac{\pi}{2}\right)}
\]

(5)
1) Oscillation Mode and Stability: Let us suppose the two oscillators are stable and oscillate at a common frequency $\omega_{osc}$. Substituting $\theta_1 = \omega_{osc} t$ and $\theta_2 = \omega_{osc} t + \varphi$ into (4) and (5), the solutions of $\varphi$ are $\varphi_1 = \pi/2$; see equation (6) at the bottom of the page, where $m$ is the coupling strength and defined as

$$m = \frac{i_{inj}}{I_{osc}} - \frac{i_{inj}}{I_0}$$

(7)

From the analysis of the previous subsection, we know that $i_{inj}$ should be less than $2I_0/\pi$, that is $0 < m < 1$. The second and third solutions are non-quadrature. The first solution indicates that the IPIC-QVCO has a phase difference of $\pi/2$ between the two oscillators. Substituting $\varphi_1 = \pi/2$ into (4) and (5) gives $d\theta_1/dt - d\theta_2/dt = -\omega_{osc}$. The result is obvious: the total injection current from the coupling network $i_{inj}$ is in phase with the oscillating current $I_{osc}$. So there is no additional phase-shift in the tank. The oscillator operates at the resonant frequency of the $LC$ tank as shown in Fig. 4(c). That is, the IPIC-QVCO is in-phase injection-coupled.

Perturbation analysis can be used to check the stability of this solution. A stable system should correct the perturbation by itself. We assume that the phases of the two oscillators have some small change due to perturbation: $\theta_1 = \omega_{osc} t + \tilde{\theta}_1$ and $\theta_2 = \omega_{osc} t + \pi/2 + \tilde{\theta}_2$, where $|\tilde{\theta}_1|,|\tilde{\theta}_2| \ll 1$. Substituting these expressions into (4) and (5) and simplifying the results, we get

$$\frac{d(\tilde{\theta}_1 - \tilde{\theta}_2)}{dt} = -\frac{\sqrt{2}g_{mK}V_i\omega_{osc}}{2QI_v(1-m)}(\tilde{\theta}_1 - \tilde{\theta}_2) = -\frac{1}{\tau}(\tilde{\theta}_1 - \tilde{\theta}_2)$$

(8)

where $\tau = \frac{\sqrt{2}QI_v(1-m)}{g_{mK}V_i\omega_{osc}}$ is the damping time-constant of the system. The larger coupling strength $m$ leads to smaller $\tau$ and a faster system in suppressing the disturbance. Since $\tau > 0$, any perturbation in the phase of the output voltage will decay, which means that this mode is unconditionally stable.

We can also apply perturbation analysis to check the stability of solutions $\varphi_{2,3}$. However, due to the complexity of the expressions, little information can be obtained from the expressions directly. We have varied the parameters within the range of all practical values for 60 GHz QVCO, and the quantitative analysis shows that the two solutions are unstable. In addition, these two solutions have not been observed in our simulation.

2) Phase Error due to Mismatches: In practical implementation, there are device mismatches in QVCOs because of the asymmetric layout or the process variation, which leads to phase error. The mismatches may exist in the $LC$ tank resonant frequency, tank quality factor, coupling network, and tail current. We suppose all the mismatches are in the second oscillator: oscillation frequency $\omega_{c2} = \omega_0 + \Delta\omega_0$, tank quality factor $Q_2 = Q + \Delta Q$, dimension of transistors in the coupling network $W_{C2} = W_{C} + \Delta W_C$, $V_i$ of transistors in the coupling network $V_{i,c2} = V_{i,c4} = V_i + \Delta V_i$, and tail current $I_{0,2} = I_0 + \Delta I_0$, which results in the phase error represented by $\Delta \varphi$. Let us assume the phase error is in the second oscillator, so its phase is $\theta_2 = \theta_1 + \pi/2 - \Delta \varphi$. Substituting all these expressions into (4) and (5) and simplifying the results, we obtain

$$\Delta \varphi = \frac{\sqrt{2}QI_v(1-m)}{g_{mK}V_i}\omega_0 + \frac{(1 - \sqrt{2}\pi V_0)}{4V_i}\frac{\Delta W_C}{W_C} + \frac{\Delta V_i}{V_i} \left(1 - \frac{\sqrt{2}\pi V_0}{4V_i}\right)$$

(9)

Similar to the P-QVCO, if the coupling strength $m$ increases or tank $Q$ decreases, the phase error of IPIC-QVCO due to $\omega_0$ mismatch decreases. Interestingly, $\tau$ also represents the suppression of phase error due to $\omega_0$ mismatch because a small $\tau$ results in a small phase error. Fig. 5 compares the real transistor simulated and calculated phase errors due to mismatches in the coupling network and $\omega_0$. The oscillation frequency is set to 60 GHz, with a tank $Q$ of 6, tail current of 5 mA, and coupling strength of 0.2. The theoretical results show good agreement with the simulation results.

It is noteworthy that, as implied by (9), the quadrature accuracy is not affected by mismatches of $Q$ and $I_v$, but by the mismatch in the coupling network. This seemingly contradictory phenomenon can be explained with voltage and current phasor diagrams. Suppose the IPIC-QVCO has quadrature outputs in the initial state with no mismatch. Mismatches of $Q$ and $I_v$ will cause the amplitude of output voltages in the second oscillator to change as depicted in Fig. 6(a). Although $V_{gs,i}$ ($i = 1,2,3,4$) and the corresponding $I_{ds,i}$ are changed, $I_{inj,i}$ is still in phase with the output voltage and $I_{osc,i}$. Therefore, the QVCO remains locked to $\omega_0$ with quadrature output phases. On the other hand, the mismatch in the coupling network will change $I_{0,2}$ and

$$\varphi_{2,3} = 2\arctan\left(\frac{1}{4g_{mK}V_i}\left(\pi g_{mK}V_0 - 2I_0 \pm 2\sqrt{I_0(1-m)(\pi g_{mK}V_i - I_0(1+m))}\right)\right)$$

(6)
Fig. 6. Voltage and current phasor diagrams due to (a) Q, Ii, and (b) coupling network mismatches.

$I_{44}$, instead of $V_{Q,4}$, as shown in Fig. 6(b). Thus, $I_{nij}$ has a phase-shift with $I_{osc}$. The different phase-shifts in the two oscillators will cause their output phases to depart from quadrature, and thus phase error appears. Fortunately, since the coupling network is simple and symmetric, the mismatch caused by the layout is small. The phase error is less than 1° within a 5% mismatch in the coupling network as depicted in Fig. 5.

3) Phase Noise: Phase noise can be analyzed as weak injection by using Alder’s equation. We treat white noise in each device as individual weak injection current into the two oscillators. The injection currents directly or indirectly lead to phase noise. By following the steps in [16], the phase noise caused by the white noise in the tank, cross-coupled pair, and coupling network can be derived from (4) and (5):

$$L(\omega_m) = \frac{k_B T \omega_0}{2 Q C V_C^2 (1 - m)^2 \omega_m^2}$$

(10)

where $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, and $\gamma$ is the MOS channel noise factor. The effective output voltage is $V_{eff} = V_0 (1 - m)$. The factor $m$ represents the ratio of current flow into the coupling network. This is similar to the P-QVCO if we merge the tail current source in the cross-coupled pair and the coupling network, because a portion of $I_0$ is consumed by the coupling network. In contrast to the phase error, the phase noise of IPIC-QVCO due to white noise increases with coupling strength and decreases with tank $Q$. Therefore, there are trade-offs in coupling strength and tank $Q$ when considering both phase error and phase noise in IPIC-QVCO design. Fig. 7 compares the simulated phase noise and calculated phase noise using (10), and the difference is less than 1.5 dB.

Flicker noise in the cross-coupled pair of a differential $LC$ oscillator contributes to negligible phase noise since it is sampled at twice the oscillation frequency [25]. However, flicker noise in the coupling network of P-QVCO introduces significant phase noise. This is because in the real circuit, the oscillation frequency of P-QVCO depends on the transconductance of the coupling network $G_{un,C}$. The flicker noise slowly modulates $G_{un,C}$ and is up-converted into the close-in $1/f^3$ phase noise [26]. In addition, the noise current injects at the zero-crossing of the output voltage, exacerbating the flicker noise up-conversion.

Fig. 7. Simulated (□) and calculated (solid line) phase noise from white noise in tank, cross-coupled pair, and coupling network.
Fig. 8. Full schematic of the proposed 60 GHz IPIC-QVCO.

Fig. 9. Simulated phase noise and phase error versus (a) coupling factor and (b) bias voltage $V_b$ in 60 GHz IPIC-QVCO.

to fully utilize the tuning characteristic of the varactor. The eight overlapped bands can cover the four required frequency spots in IEEE 802.15.3c with low VCO gain ($K_{\text{VCO}}$).

The passive devices such as inductors and transmission lines are all custom designed. Since the parasitics of interconnects and devices play important roles in the mm-wave circuit design, we use an electromagnetic (EM) simulator to obtain their S-parameters. The S-parameters files are then sent back to Cadence SpectreRF for circuit simulation with active devices. Because the $f_1/f_{\text{max}}$ of 65 nm transistors are sufficient high for 60 GHz application, the model described in the previous subsection is valid as long as the tank or S-parameters files take the parasitics of interconnects and devices into account.

As mentioned previously, there is a trade-off between phase noise and phase error in terms of the coupling strength $m$. We can choose a proper $m$ and power to meet the phase noise and phase error requirements simultaneously. However, to get a particular $m$ is tedious for the mm-wave circuit design, because it is difficult to distinguish the currents flowing into the transistors and their parasitics. A more efficient method for mm-wave circuit design is through simulation iterations. We define the coupling factor $\alpha$ as the ratio of the transistor’s width in the coupling network to the transistor’s width in the cross-coupled regenerative pair. Note that in IPIC-QVCO, $m$ is determined by the coupling factor $\alpha$ and the bias voltage $V_b$. Simulations are carried out to find the optimum values of $\alpha$ and $V_b$. We choose $f_0 = 60$ GHz, $M_R = 20 \mu m/6.06 \mu m$, $L = 60 \mu H$, $Q_L = 15$, $I_0 = 51 mA$. Fig. 9 shows the simulated phase noise and phase error by varying $\alpha$ and $V_b$. We note that the phase error is small and does not change much if $\alpha > 0.5$ and $V_b > 0.3 V$. So the coupling network without $V_b$, which is used in our QPLL, can achieve good performance. In our design, to ensure the start-up and the wide tuning range under the process and temperature variation, a small coupling network is chosen. $W_R$ is set to 20 $\mu m$, and $\alpha$ is chosen as 1/3.

We also compare IPIC-QVCO with other conventional QVCOs: P-QVCO, bottom series QVCO [29], superharmonic-coupled QVCO [30], and magnetically-coupled QVCO [17]. Unless otherwise stated, all the conditions are the same. The simulated performances are summarized in Table I. Compared with other conventional QVCOs, the IPIC-QVCO has large output amplitude, good phase noise, and good phase error. Moreover, the IPIC-QVCO exhibits good performance at multi-GHz frequencies in our simulation.
TABLE I
SIMULATED PERFORMANCES OF 60 GHZ IPIC-QVCO AND OTHER CONVENTIONAL QVCOS

<table>
<thead>
<tr>
<th>Prototype</th>
<th>Oscillation Amplitude (Vp)</th>
<th>Phase Noise @1MHz (dBc/Hz)</th>
<th>Phase Error (0.1% capacitance mismatch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-QVCO [34] (α=1)</td>
<td>0.25</td>
<td>-78.0</td>
<td>0.04°</td>
</tr>
<tr>
<td>P-QVCO (α=1/3)</td>
<td>0.41</td>
<td>-87.9</td>
<td>0.3°</td>
</tr>
<tr>
<td>Bottom series QVCO [29] (α=3.5)</td>
<td>0.38</td>
<td>-86.8</td>
<td>0.2°</td>
</tr>
<tr>
<td>Superharmonic-coupled QVCO [30]</td>
<td>(k=0.5, α=0.02)</td>
<td>0.61</td>
<td>-94.4°</td>
</tr>
<tr>
<td>Magnetically-coupled QVCO [17]</td>
<td>(α=0.15, L=100pH)</td>
<td>0.42</td>
<td>-94.1°</td>
</tr>
<tr>
<td>IPIC-QVCO (α=1/3)</td>
<td>0.46</td>
<td>-97.0</td>
<td>0.6°</td>
</tr>
<tr>
<td>IPIC-QVCO (α=1)</td>
<td>0.4</td>
<td>-95.4</td>
<td>0.3°</td>
</tr>
</tbody>
</table>

Fig. 10. (a) Schematic, (b) simulated locking range and (c) waveforms of the modified DCML divide-by-4 divider.

III. DIVIDER CHAIN AND CHARGE PUMP DESIGN

A. Low Power Inductor-Less Divider Chain

Designing frequency dividers is challenging in mm-wave PLL since they may consume substantial power. Large area is another issue due to the use of inductors. In this work, the inductor-less DCML divider, ILFD, and TSPC divider are implemented in cascade. By using these divider topologies, the low power and small area can be achieved simultaneously. We will describe them separately.

Fig. 10(a) depicts the schematic of the modified DCML divide-by-4 frequency divider. Compared with a traditional CML divider, the DCML divider uses the parasitic capacitor in differential amplifier pair, instead of a static cross-coupled latch, to store the data [21]. By removing the cross-coupled pairs, the maximum operation frequency of the divider is increased, making it suitable for mm-wave frequency. To further improve its performance, two methods have been adopted. Firstly, low threshold voltage (low-Vt) devices are used to increase the maximum operation frequency for their higher fT. Secondly, we merge the switches of the same input clock of the DCML divider in [21], i.e., node XA and node XR are connected together. By connecting XA and XR, we now present a balanced and high conductance point at the input frequency. Therefore, the injection currents of the modified DCML divider are larger than that of the conventional DCML divider, as shown in Fig. 10(c). From the point of view of injection locking, the locked bandwidth of the modified DCML divider is enlarged. In order to balance the output loadings, all the eight-phase outputs of the DCML divider serve as the inputs of the next divider. Fig. 10(b) shows its post-layout simulation results with different bias voltages VDD. With about 300 mV peak-to-peak input voltage, the divider works from 35 GHz to 77 GHz, with at least 3 GHz bandwidth in each sub-band. Thus, two sub-bands can cover the four frequency spots of IEEE 802.15.3c. The simulated power consumption is about 9.0 mW at 60 GHz frequency, at a 1.2 V supply.

Fig. 11(a) depicts the schematic of the injection-locked divide-by-4 divider. Its eight-phase inputs are from the outputs of the DCML divider. Each two adjacent phase inputs are added through transistors to generate four injection currents. The four injection currents are in quadrature with enhanced amplitude as shown in Fig. 11(b). The multiphase injection with proper sequence can improve the locking range of the divide-by-4 ILFD...
Fig. 11. (a) Schematic, (b) phasor of injection current, and (c) simulated locking range of the injection-locked divide-by-4 divider.

[31]. Fig. 11(c) shows its post-layout simulation results with different bias voltages $V_{BIP}$. With about 300 mV peak-to-peak input voltage, the divider works from 8 GHz to 28 GHz. The locking range of each sub-band is large enough to cover about 5 GHz input range. The simulated power consumption is less than 3.2 mW with a 1.2 V supply.

The multi-modulus divider consists of four divide-by-2/3 TSPC divider cells and one control circuit. It can realize the four-division modulus (27, 28, 29, and 30) with low power consumption. The output of the multi-modulus divider is taken from the first divide-by-2/3 divider to reduce the phase noise, because it is retimed by the high frequency input. The simulated power consumption is about 0.7 mW.

B. Low Spur Charge Pump

The programmable self-correcting low spur CP, shown in Fig. 12(a), is modified from [32]. The voltage-to-current (VI) converter, which includes a rail-to-rail amplifier, senses the voltage difference between $V_1$ and $V_2$, and corrects the mismatch between charge and discharge currents. Thus, the static phase offset is minimized and the effective tuning range is maximized. However, there are two problems in [32]: clock feedthrough and charge injection in the switches. In our proposed charge pump, two measures are taken to avoid these two problems and further reduce spurious level. First, the UP/DN switches are moved to the source of current source transistors to eliminate the clock feedthrough and charge injection. Second, the VCO control voltage $V_{ctl}$ is connected to $V_1$, instead of $V_2$. So $V_1$ can be regarded as $V_2$ after a unity-gain amplifier. The benefit is that the ripple in $V_2$ caused by the reference clock can be filtered by this follower as long as its bandwidth $f_{amp}$ is less than the reference frequency $f_{ref}$. It also isolates the switches and $V_1$, so the clock has negligible effect on the output. On the other hand, $f_{amp}$ is designed to be significantly larger than the PLL loop bandwidth $f_{PLL}$, to minimize the effect on the system loop characteristics and stability. In this design, $f_{PLL}$ can be programmed from 0.5 to 2 MHz, and $f_{ref}$ and $f_{ctl}$ are about 40 and 135 MHz, respectively. Fig. 12(b) depicts the simulated waveforms of $V_{ctl}$ when it is connected to $V_1$ and $V_2$ respectively. As expected, the amplifier does not interfere with the locking process. The ripple of $V_{ctl}$ connected to $V_1$ is much smaller, and is reduced by about 10 times compared with the one connected to $V_2$. We also performed a transient simulation to observe the reference spur levels with non-idealities: 10% charge/discharge current mismatch and 1 $\mu$A leakage current in the LPF as shown in Fig. 12(c). When $V_{ctl}$ is connected to $V_1$, the reference spur is consistently reduced by about 10 dB compared with when $V_{ctl}$ is connected to $V_2$. The simulated power consumption of this charge pump is about 0.3 mW.

IV. EXPERIMENTAL RESULTS

A 60 GHz standalone IPIC-QVCO and a 60 GHz PLL are implemented in GLOBALFOUNDRIES standard 65 nm low power CMOS technology. Fig. 13 shows the die micrograph of the standalone QVCO and the complete PLL, which occupy 0.26 $\times$ 0.15 mm² and 0.32 $\times$ 0.60 mm², respectively. The standalone IPIC-QVCO consumes 11.4 mW (not including output buffers) from a 1.2 V supply. The measured VCO tuning curves are shown in Fig. 14. The eight bands of the QVCO cover a frequency range of 57.88 to 68.33 GHz, i.e., 16.6% around the center frequency, with a tuning sensitivity less than 2 GHz/V. As depicted in Fig. 15, the measured QVCO phase noises for a 62.66 GHz carrier are -94.2 and -115.0 dBc/Hz at 1 and 10 MHz offset, respectively. The corner frequency between the $1/f^3$ and $1/f^2$ region is less
than 2 MHz, demonstrating a low flicker noise up-conversion. Note that the corner frequency can be further reduced if the size of the diode-connected transistors in the coupling network is larger. We also measured the phase noise performance across the tuning range from six samples. The phase noise is between $-92$ and $-95$ dBc/Hz at 1 MHz offset. The Figure of Merit (FOM) and FOM$_T$ are $-178.1$ to $-179.7$ and $-182.5$ to $-184.1$ dBc/Hz at 1 MHz offset, respectively. The phase and amplitude errors are measured by down-converting the quadrature signals to about 250 MHz. Fig. 17 shows that the phase error is less than $0.7^\circ$ and the amplitude error is less than 0.9 dB across 6 samples for $V_o$ at 0.6 V. To verify the characteristics of the in-phase coupling, we measure the IPIC-QVCO by varying the bias voltage $V_b$, as depicted in Fig. 18. Measurement results show that the frequency is almost constant when $V_b$ increases, indicating the coupling is in phase. The phase noise increases and the phase error decreases while the coupling strength becomes stronger, which coincides with the analysis results. Table II shows the summarized measurement results and a comparison with other state-of-the-art 60 GHz CMOS QVCOS. The proposed IPIC-QVCO has good phase noise and small phase error, and consumes the least power.

The PLL consumes 24.6 mW (not including open-drain output buffers) from a 1.2 V supply, of which, about 11.4, 12.7, and 0.5 mW are consumed by QVCO, divider chain and other blocks, respectively. The operation range of the PLL is from 57.9 to 68.3 GHz. When the reference input $f_{ref} = 135$ MHz, the PLL can be locked to the four frequencies defined by the IEEE 802.15.3c standard: 58.32, 60.48, 62.64, and 64.80 GHz. As shown in Fig. 19, PLL phase noise is $-91.0$ dBc/Hz at 1 MHz offset from a 62.64 GHz carrier. Phase noise contributors are also plotted in Fig. 19 through a combination
TABLE II
COMPARISON OF STATE-OF-THE-ART 60 GHz CMOS QVCOS

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Tech.</th>
<th>Supply Voltage (V)</th>
<th>Freq. Tuning Range (GHz)</th>
<th>Phase Noise @1MHz (dBc/Hz)</th>
<th>FOM&lt;sup&gt;a&lt;/sup&gt; (dBc/Hz)</th>
<th>FOM&lt;sub&gt;T&lt;/sub&gt;&lt;sup&gt;b&lt;/sup&gt; (dBc/Hz)</th>
<th>Phase Error</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[13]</td>
<td>45 nm</td>
<td>1.1</td>
<td>57 ~ 66 (14.5%)</td>
<td>-75&lt;sup&gt;c&lt;/sup&gt;</td>
<td>-156.3</td>
<td>-159.6</td>
<td>n.a.</td>
<td>28</td>
</tr>
<tr>
<td>[17]</td>
<td>65 nm</td>
<td>1.0</td>
<td>56.0 ~ 60.4 (7.6%)</td>
<td>-95 ~ -97</td>
<td>-177 ~ -179</td>
<td>-174.6 ~ -176.6</td>
<td>&lt;1.5&lt;sup&gt;c&lt;/sup&gt;</td>
<td>22</td>
</tr>
<tr>
<td>[35]</td>
<td>65 nm</td>
<td>1.2</td>
<td>57.5 ~ 63.1 (9.3%)</td>
<td>-95.3</td>
<td>-174.9</td>
<td>-174.3</td>
<td>n.a.</td>
<td>36</td>
</tr>
<tr>
<td>[36]</td>
<td>65 nm</td>
<td>1.2</td>
<td>54.0 ~ 61.0 (24.3%)</td>
<td>-90.0 ~ -94.0</td>
<td>-173 ~ -176</td>
<td>-181 ~ -184</td>
<td>n.a.</td>
<td>15.6</td>
</tr>
<tr>
<td>This Work</td>
<td>65 nm</td>
<td>1.2</td>
<td>57.88 ~ 68.33 (16.6%)</td>
<td>-92 ~ -95</td>
<td>-178.1 ~ 179.7</td>
<td>-182.5 ~ 184.1</td>
<td>&lt;0.7&lt;sup&gt;c&lt;/sup&gt;</td>
<td>11.4</td>
</tr>
</tbody>
</table>

<sup>a</sup> FOM = \( L\{\Delta f\} + 20\log(\Delta f/f_0) + 10\log(\text{Power/1mW})\).

<sup>b</sup> FOM<sub>T</sub> = \( L\{\Delta f\} + 20\log(\Delta f/f_0)\) (FTR/10) + 10\log(\text{Power/1mW})

<sup>c</sup> PLL phase noise.

---

Fig. 14. Measured tuning range of the IPIC-QVCO.

Fig. 15. Measured phase noise of the IPIC-QVCO.

The measured QVCO and PLL performance are summarized and compared with state-of-the-art works in Table III. Our PLL has a simple structure and can achieve good performance with ultra-low power consumption.

V. CONCLUSION

A low power fully integrated 60 GHz quadrature PLL is reported. Through a particular symmetrical coupling network, the in-phase coupling is realized in the proposed IPIC-QVCO, which reduces both phase noise and phase error. Implemented in standard 65 nm low power CMOS technology, the PLL operates from 57.9 to 68.3 GHz with 24.6 mW power consumption. PLL phase noise is from \(-89.8\) to \(-91.0\) dBc/Hz at 1 MHz offset across the frequency band. The reference spur is less than \(-54.5\) dBc. This work supports IEEE 802.15.3c and other compatible 60 GHz standards. To the authors’ knowledge, our work has the least power consumption in reported quadrature frequency synthesizers for IEEE 802.15.3c and other compatible 60 GHz standards. The IPIC-QVCO shows great potential for high performance QVCOs in both low frequency and mm-wave applications.

APPENDIX

This Appendix shows the derivation of the drain current amplitude of a diode-connected transistor at fundamental frequency. Fig. 22 shows the gate-source voltage \(V_{gs}\) and the
TABLE III

<table>
<thead>
<tr>
<th>Ref.</th>
<th>CMOS Tech.</th>
<th>Supply Voltage (V)</th>
<th>Ref. Freq. (MHz)</th>
<th>Freq. Tuning Range (GHz) (FTIR%)</th>
<th>Phase Noise @1MHz (dBc/Hz)</th>
<th>Ref. Spur (dBc)</th>
<th>Topology</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>90 nm</td>
<td>0.7 / 1.2</td>
<td>117</td>
<td>59.6 ~ 64.0 (7.1%)</td>
<td>-72.5</td>
<td>-23</td>
<td>30 GHz PLL + 60 GHz Hybrid</td>
<td>76.3</td>
</tr>
<tr>
<td>[7]</td>
<td>65 nm</td>
<td>1.0 / 1.2</td>
<td>36</td>
<td>54 ~ 61 (12.2%)</td>
<td>-94.2</td>
<td>n.a</td>
<td>20 GHz PLL + 60 GHz QILO</td>
<td>80.9</td>
</tr>
<tr>
<td>[9]</td>
<td>40 nm</td>
<td>1.1</td>
<td>20000</td>
<td>55 ~ 66 (18.2%)</td>
<td>&lt; -96</td>
<td>n.a</td>
<td>60 GHz QILO QPLL</td>
<td>112</td>
</tr>
<tr>
<td>[13]</td>
<td>45 nm</td>
<td>1.1</td>
<td>100</td>
<td>57 ~ 66 (14.6%)</td>
<td>-75</td>
<td>-42</td>
<td>60 GHz QPLL</td>
<td>78</td>
</tr>
<tr>
<td>[37]</td>
<td>40 nm</td>
<td>1.1</td>
<td>n.a.</td>
<td>63 ~ 70 (10.5%)</td>
<td>-85</td>
<td>&lt; -40</td>
<td>60 GHz QPLL</td>
<td>66</td>
</tr>
<tr>
<td>This Work</td>
<td>65 nm</td>
<td>1.2</td>
<td>135</td>
<td>57.9 ~ 60.3 (16.5%)</td>
<td>-89.8</td>
<td>-54.5</td>
<td>60 GHz QPLL</td>
<td>24.6</td>
</tr>
</tbody>
</table>

(a) QILO = Quadrature injection-locked oscillator.

Fig. 17. Measured phase and amplitude errors of the IPIC-QVCO when \( V_{th} = 0.6 \) V.

Fig. 18. Measured output frequency, phase noise at 1 MHz offset, and phase error versus bias voltage \( V_{th} \) in the IPIC-QVCO.

The transistor is turned on when \( V_{gs} > V_{th} \), so the total conduction angle \( 2\Phi \) is

\[
2\Phi = 2 \arccos \left( \frac{V_{th}}{2V_0 \sin \frac{\varphi}{2}} \right)
\]

where \( 2 \arcsin \left( \frac{V_{th}}{2V_0} \right) < \varphi < 2\pi - 2 \arcsin \left( \frac{V_{th}}{2V_0} \right) \), to ensure the transistor is turned on and works in saturation region.

In a modern transistor, when \( V_{th} \) is larger than saturation drain voltage \( V_{ds,sat} \), the carrier drift velocity saturates. In a diode-connected transistor, the saturation region meets this condition because usually \( V_{ds,sat} < V_{th} \). Therefore, the drain current is given by [33]

\[
I_d = g_{mK} (V_{gs} - V_{th}) = g_{mK} \left( 2V_0 \sin \frac{\varphi}{2} \cos \omega t - V_{th} \right)
\]

where \( g_{mK} = K V_{th,sat} C_{ox} W \), \( K \) is the short-channel effect modeling parameter and \( V_{th,sat} \) is the saturation velocity of a transistor.

Since we assume the tank \( Q \) is high enough, only the fundamental current is considered. The fundamental term of \( I_d \) in the Fourier series is computed as follows:

\[
i_d = \frac{\omega}{\pi} \int_{-\varphi/\omega}^{\varphi/\omega} g_{mK} \left( 2V_0 \sin \frac{\varphi}{2} \cos \omega t - V_{th} \right) \cos \omega t dt
\]

\[
= \frac{g_{mK}}{\pi} \left( V_0 \sin \frac{\varphi}{2} (2\Phi + \sin 2\Phi) - 2V_{th} \sin \Phi \right).
\]
Substituting (12) and using the series of \( x = \pi / 2 - x - x^3 / 6 + \cdots \) for \( 2 \arcsin \left( \frac{V_i}{2V_0} \right) < \varphi < 2\pi - 2 \arcsin \left( \frac{V_i}{2V_0} \right) \), we can simplify (14) as

\[
i_\pi(\varphi) \approx g_m \left( \frac{V_0}{2} \sin \frac{\varphi}{2} - \frac{2}{\pi} V_i \right).
\]

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REFERENCES

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