A 10–67 GHz 1.44 mW 20.7 dB Gain VGA-Embedded Downconversion Mixer with 40 dB Variable Gain Range

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Abstract—A high gain low power variable gain downconversion mixer is presented here. In a conventional mixer, its conversion gain is limited by the load impedance due to limited voltage supply. In addition, accurate conversion gain control is challenging due to DC-offset and various parasitic effects.

By using a negative resistance to negate the load resistance and implementing a DC free variable resistor across the output, the seemingly fundamental limitation mentioned above can be eliminated. This way, high gain mixer with controllable variable gain can be achieved at low voltage supply. Thus, variable-gain amplifier (VGA) can be removed in a receiver to save power.

The measured conversion gain is 16.5 to 20.7 dB over the operation frequency of 10 to 67 GHz. Furthermore, the measured variable gain range is 40 dB at 24 GHz. To the best of the authors’ knowledge, this is the first millimeter-wave (mm-wave) variable gain CMOS mixer ever reported. In addition, this work also demonstrates the highest conversion gain among all CMOS mm-wave active mixers with the least power consumption.

Index Terms—Low power, high conversion gain, variable-gain amplifier (VGA), downconversion, millimeter-wave, mixer, CMOS.

I. INTRODUCTION

Thanks to the advance in CMOS technology, high integration low cost millimeter-wave (mm-wave) systems, such as 60 GHz high data rate communication, 24/77 GHz automotive radar, and 94 GHz mm-wave imaging, are demonstrated in recent years. Most mm-wave applications cover wide frequency bands, leading to the requirement of wideband mm-wave transceivers. One of the essential components in the receiver is the downconversion mixer. For a fixed voltage supply, there are tradeoffs between conversion gain, linearity, noise figure, and power consumption in a conventional downconversion mixer. The conversion loss of a passive mixer is high in mm-wave frequency [1-3]. Similarly, the power hungry conventional active mixer suffers from low conversion gain at mm-wave frequency [4-6], which increases the noise figure requirement of the following stages. Typically, a variable-gain amplifier (VGA) should be used after the mixer in a receiver to improve the overall gain range. However, the DC-offset at the output of the mixer is a critical issue for the VGA design. Additional DC-offset cancellation techniques should be employed to solve this problem, which increases the design complexity and power.

In this letter, a low voltage low power VGA-embedded downconversion mixer is proposed as shown in Fig. 1. Controllable conversion gain with high conversion gain and large gain range are achieved simultaneously. Since the VGA is embedded, the VGA’s related problem mentioned above vanishes, and the total power is reduced. The analysis of the proposed design will be discussed in Section II. Measurement results will be shown in Section III. Finally, the conclusion is made in Section IV.
II. ANALYSIS OF PROPOSED DESIGN

Before explaining the proposed mixer, let us firstly describe the conventional downconversion mixer. Fig. 2(a) shows the schematic of a conventional single-balance downconversion mixer. The radio frequency (RF) input $V_{RF}$ is applied at the gate of the amplifying transistor (M1), and converted into current $I_{RF}$, as illustrated in Fig. 2(b). $I_{RF}$ is commutated by local oscillator (LO) voltage $V_{LO}$ through the switching transistors M1 and M2, and downconverted to intermediate frequency (IF) current $I_{IF}$. Finally, the current $I_{IF}$ is converted into the output voltage $V_{IF}$ through $R_D$. The conventional downconversion mixer exhibits very low conversion gain at mm-wave frequency. One reason is that, a portion of $I_{RF}$ flows to ground through the parasitic capacitor $C_p$ at node X at mm-wave frequency. More importantly, the conversion gain is proportional to load resistor $R_D$, however, the latter is limited by the voltage headroom and to ensure good linearity.

In order to improve the conversion gain, two measures are taken in the proposed mixer as shown in Fig. 3. Firstly, $V_{RF}$ is applied to node X through a transmission line and an AC coupled capacitor $C_p$. $C_p$ is now a part of matching network, so most of $I_{RF}$ will flow into the switches. Secondly, the cross-coupled pair, M2 and M3, is implemented to provide a negative resistance that enhanced the conversion gain [7].

The proposed mixer not only has high conversion gain, but also the convenience of gain control, which makes it to have the function of a VGA. A variable resistor $R_{var}$ is placed in parallel to $R_p$ var, and its value obtained from post-layout simulation is from 10 Ω to infinity. By extension, the NMOS transistor can also be replaced with an array of switched resistors to achieve a digitally-controlled resistance for linear gain variation.

III. EXPERIMENTAL RESULTS

The proposed mixer is implemented in GLOBAL-FOUNDRIES 65 nm CMOS technology. The die photograph is shown in Fig. 4. The area of mixer including pads is about 700 $\mu$m × 420 $\mu$m, and the active core circuit occupies only 25 $\mu$m × 30 $\mu$m. The core circuit consumes about 1.31-1.69 mW from 1.2 V supply. The buffer is designed for measurement with about 0 dB voltage gain at 100 MHz IF.

The conversion gain is measured by applying the RF signal using Agilent N5247A network analyzer and measuring the IF output through a spectrum analyzer. Fig. 5 shows the measured conversion gain versus LO power when RF is 24 GHz from four dies. As mentioned previously, the conversion gain can be varied through $R_{var}$. The maximum conversion gain is 20.7 dB when LO power is -2.5 dBm. The conversion gain degrades with IF output impedance when LO power is larger than 0 dBm. By varying $R_{var}$, 40 dB conversion gain range is achieved.

The simulated and measured conversion gains versus RF frequency and measured RF port S11 are depicted in Fig. 6. In simulation, the conversion gain is larger than 17 dB when RF is from 10 to 100 GHz. In measurement, the measured conversion gain is higher than 16.5 dB when its operation frequency is from 10 to 67 GHz. The conversion gain variations are within 3 dB at frequency between 10 and 67 GHz, and are within 2 dB at 24 GHz from four dies. The variations mainly come from the mismatches between $R_p$ and $1/g_{out}$, as described in (1). However, the variable gain range is about 40 dB and the variation mentioned above can be compensated by varying $R_{var}$. The RF port return loss is larger than 6 dB when RF frequency is from

![Fig. 4. Die photograph of the proposed mixer.](image-url)
10 to 67 GHz. The measured operation frequency is limited by the equipment.

Table I

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology</th>
<th>$V_{DD}$ (V)</th>
<th>RF Frequency (GHz)</th>
<th>Conversion Gain (dB)</th>
<th>OIP3 (dBm)</th>
<th>NF (dB)</th>
<th>Power (mW)</th>
<th>Notes</th>
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<td>[1]</td>
<td>CMOS 90 nm</td>
<td>-</td>
<td>9 – 31</td>
<td>-8</td>
<td>-5</td>
<td>-</td>
<td>0</td>
<td>Passive</td>
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<td>-</td>
<td>16 – 46</td>
<td>-13</td>
<td>1</td>
<td>17.4</td>
<td>0</td>
<td>Passive</td>
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<tr>
<td>[3]</td>
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<td>-</td>
<td>0.8 – 77.5</td>
<td>-4.5 – 6.5</td>
<td>-</td>
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<td>0</td>
<td>Passive</td>
</tr>
<tr>
<td>[4]</td>
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<td>3.3</td>
<td>9 – 50</td>
<td>5 – 12</td>
<td>4.8 – 11.8</td>
<td>16.4</td>
<td>97</td>
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<td>25 – 75</td>
<td>1 – 5</td>
<td>12 – 16</td>
<td>-</td>
<td>93</td>
<td>Gilbert-Cell</td>
</tr>
<tr>
<td>[6]</td>
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<td>3.3</td>
<td>30 – 100</td>
<td>-3 – 0</td>
<td>-</td>
<td>-</td>
<td>58</td>
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<td>[7]</td>
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<td>1.2</td>
<td>77</td>
<td>6.8</td>
<td>-</td>
<td>21</td>
<td>3</td>
<td>Narrowband</td>
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<td>1.2</td>
<td>10 – 67</td>
<td>16.5 – 20.7</td>
<td>0 – 4</td>
<td>16.5 – 20**</td>
<td>1.31–1.69</td>
<td>40dB variable gain range</td>
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</table>

* Limited by measurement equipment.
** Simulated results.

Fig. 5. Measured conversion gain versus LO power when $R_{var}$ increases at 24 GHz from four dies.

IV. CONCLUSION

In this letter, we propose a 10-67 GHz 20.7 dB gain VGA-embedded downconversion mixer with 40 dB variable gain range. By introducing the negative resistance and an additional variable resistor, the conversion gain and its gain range are improved. A prototype is implemented in 65 nm CMOS technology with very low power consumption.

REFERENCES
