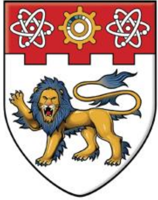

School of Electrical & Electronic Engineering

17 September 2009

EEE teams up with IME & IHPC to form Singapore 3D Through-Silicon Via (TSV) Consortium

3D integration is identified as a key and promising path, not only to facilitate the continuation of the conventional scaling (More Moore), but also to enable heterogeneous integration (More-than-Moore) of vast different functionalities above integrated circuits. In wafer level 3D integration, full or partial integrated circuits are usually bonded and electrically interconnected by through-silicon-via (TSV). NTU, as a core member in this Singapore 3D TSV Consortium led by IME, will play a key role in research and development of TSV in Phase I and more advanced enabling technology in Phase II. This effort is led by the School of Electrical and Electronic Engineering. Research on 3D integration is one of the key activities in the Silicon Nanoelectronics Group in the Microelectronics Center at EEE, and the participation in this consortium will enable direct interaction with industry to explore, identify, develop, and refine enabling technology for realization of future 3D integrated circuits.

More details: A*STAR AND EDB LAUNCH 3-DIMENSIONAL THROUGH-SILICON VIA CONSORTIUM TO BOOST NEXT GENERATION WAFER MANUFACTURING CAPABILITY FOR SINGAPORE SEMICONDUCTOR INDUSTRY