

The Virtual Wafer Fab Technology for the Deep-Submicron ULSI Era

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Abstract

*This article describes a new technology, the virtual wafer fab technology, which has become increasingly popular in the semiconductor industry for the deep-submicron era. The first section, **Introduction**, which is taken from the author's lecture notes for the 4th-year design course, is intended for readers who are not familiar with the field. The second section is on the motivation and ideas of the **Virtual Wafer Fab** and some related concepts. The last section describes an on-going joint project with the local wafer fab, **Project DOUST**, its goals, ideas, and potential impact.*

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INTRODUCTION

Have you ever imagined this: Whenever you push the button of an electronic system (e.g., the keyboard of a computer, or the remote control of a VCR), you are actually manipulating the motion of individual electrons inside the system.

Since the invention of the transistor 50 years ago and the advent of the modern VLSI technology, we have witnessed the dramatic advancement in the microelectronics industry. It is all based on the foundation of the semiconductor industry for our ability to make electrons move faster, transistors smaller, and more transistors on a single chip. As this trend leads us into the ultra-large-scale integration (ULSI) era, the deep-submicron technology calls for new design methodologies and new electronic design automation (EDA) tools to cope with the complexity and coupling among different stages of a design.

Spectrum of Approaches to Analyzing Microelectronic Systems

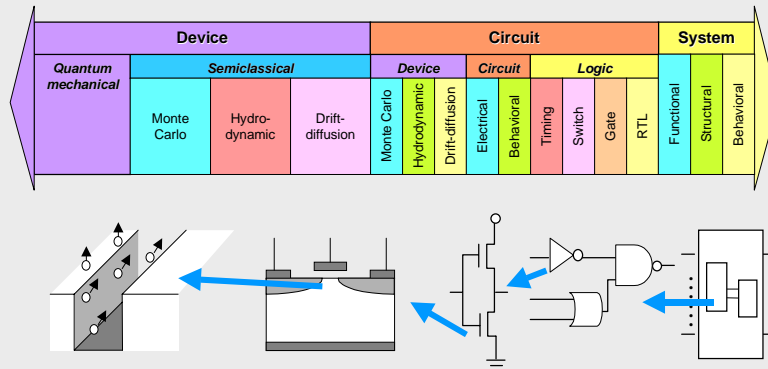
There exists a wide spectrum of approaches to analyzing microelectronic systems, which can be largely classified into three levels: *system*, *circuit*, and *device*, with the corresponding three walks of people: system designers, circuit engineers, and device physicists.

At the “engineering end” of the spectrum, system designers are concerned with the behavior and functionality of a complex system. In general, a top-down synthesis approach is employed in a system design. Design methodologies evolve with the rapid advancement of the technology as well as design tools. New approaches, such as semi-custom design (standard cell, gate array, field-programmable gate array, etc.) for the application-specific integrated circuits (ASIC), have been widely used. Nowadays, it is totally unimaginable that a Pentium chip can be “designed” bottom-up without the use of advanced EDA tools.

Traditionally, integrated circuit design has been centered at the *de facto* industry standard — the Berkeley SPICE circuit simulator. Higher-level logic simulators (such as switch-level timing analyzers, gate-level or register-transistor-level simulators) are aimed at increased simulation speed at the expense of accuracy. On the other hand, circuit designers expect a set of SPICE parameters to be extracted from the lower layout or technology level for use in circuit simulation as well as logic-level verification.

For ultra-small-size transistors or non-steady-state transport problems, the closed-form macromodels at the circuit level will not be sufficient or valid for the analysis of the problem at hand. Device electrical performance is characterized by 2D/3D numerical solutions of the coupled Poisson and current continuity equations, together with the drift-diffusion (DD) or energy-balance (EB) equations. When highly nonequilibrium and nonlocal effects are of importance, Monte Carlo (MC) technique is used to solve for the exact solution of the Boltzmann transport equation. Finally, at the “physics end” of the spectrum, many attempts have been made to formulate a rigorous theory of quantum transport.

Spectrum of Approaches to Analyzing Microelectronics Systems



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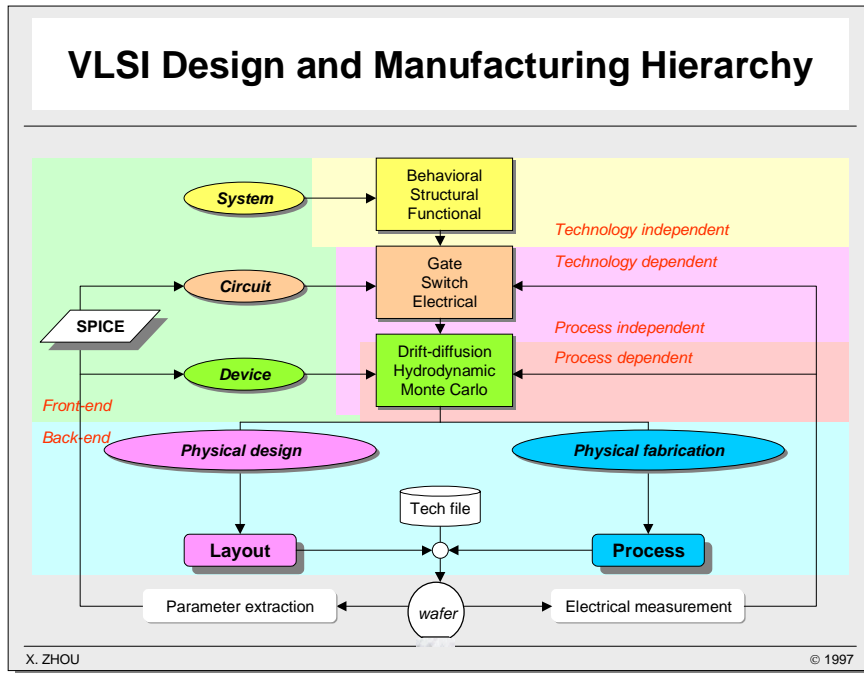
VLSI Design and Manufacturing Hierarchy

A microelectronic system, from concept to product, must go through the process of design and implementation. Before the deep-submicron era, a full-custom design (as opposed to other semi-custom ASICs) mainly consists of two sessions: *frontend* and *backend*.

In frontend design, it usually starts from the *system level* with a top-down synthesis approach, which is technology independent (i.e., at this level, it is “irrelevant” whether the design will be implemented in CMOS or bipolar technology). The design is then transformed into the *circuit level*, in which the logic functionality, timing delays, speed and power, etc., are the primary concerns. This level is technology dependent but relatively process independent. If more detailed study on the transistor performance is needed, it can be supplemented at the *device level* based on the device physics which, in general, requires process information.

At the backend, the final design must be translated into the physical layout representation, which is to be used to implement in wafer fabrication. In the “conventional” hierarchy, technology development (manufacturing) is relatively independent of the design. The “feedback” only occurs at the circuit level where the fab provides the circuit designer a set of SPICE parameters for the particular process through electrical measurement and parameter extraction of the fabricated transistors.

From the described VLSI design and manufacturing hierarchy, two streams of knowledge can be identified: vertically, a single design is represented at different levels of abstraction; horizontally, any design (in its final layout format) must be combined with a process recipe to be implemented, step by step, on a silicon chip.



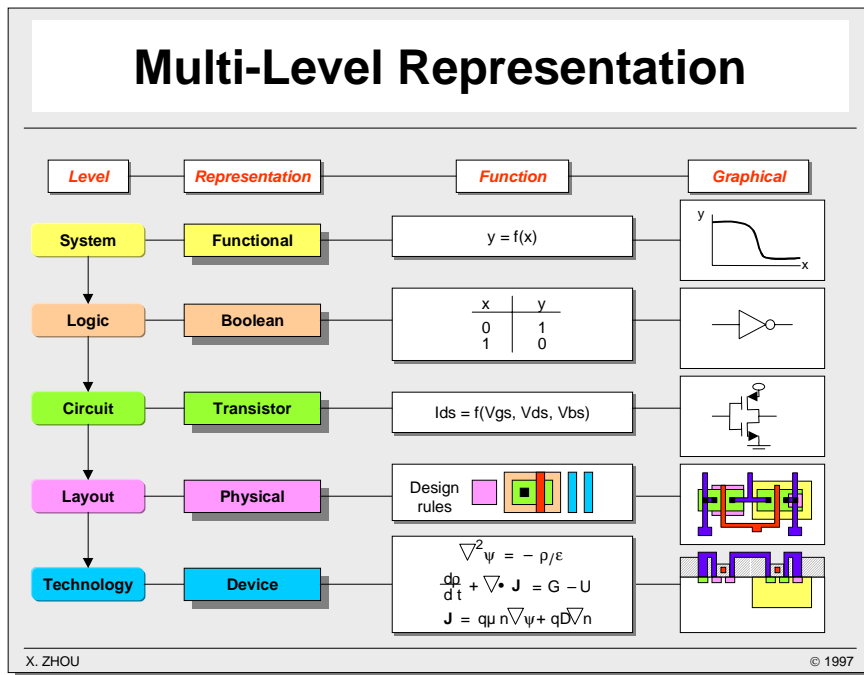
Multi-Level Representation

The design and implementation of an integrated circuit, be it the whole system on a chip or a single inverter, can be represented at five distinctively different levels of abstraction (take the inverter as an example):

- **System level:** *functional representation* where the behavior of the system is described by its transfer function;
- **Logic level:** *Boolean representation* where the system is represented by its logic function plus some limited modeling of the propagation delays;
- **Circuit level:** *transistor representation* where the system is characterized by closed-form nonlinear equations for each transistor I–V characteristics;
- **Layout level:** *physical representation* where the system is drawn by its equivalent geometric patterns subject to the given design rules;
- **Technology level:** *device representation* where the system is simulated by a set of physical differential equations on the cross-sectional plane of its final structure.

You may ask why there are so many levels of representations for the same design. The answer is that for a complex problem, a “divide-and-conquer” approach should be used. Since an integrated circuit is designed and implemented in a hierarchical way, it should also be analyzed and simulated at different levels of abstraction. The essence of modeling is what Albert Einstein described:

“Everything should be made as simple as possible, but not any simpler.”



Layout + Process = Chip

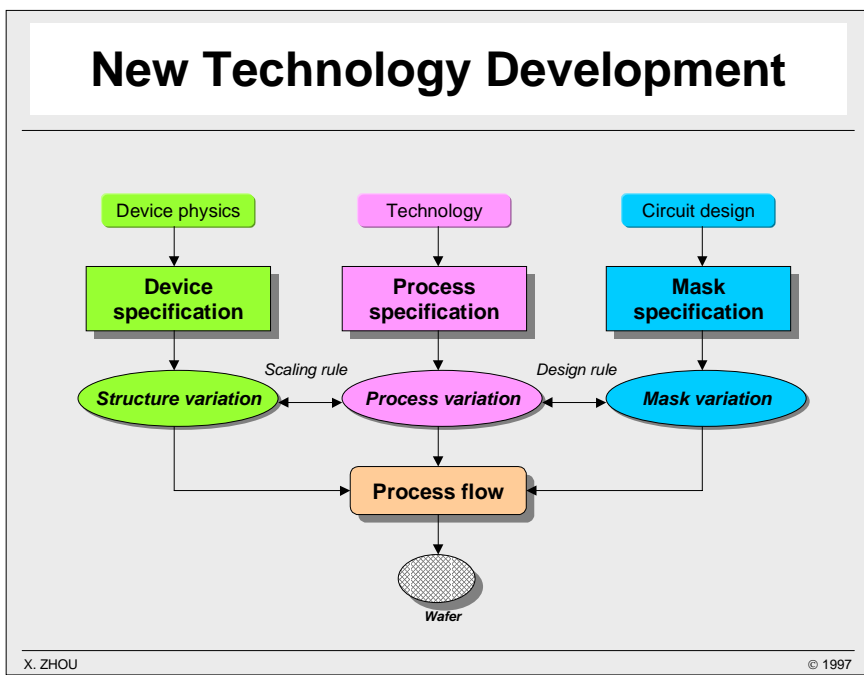
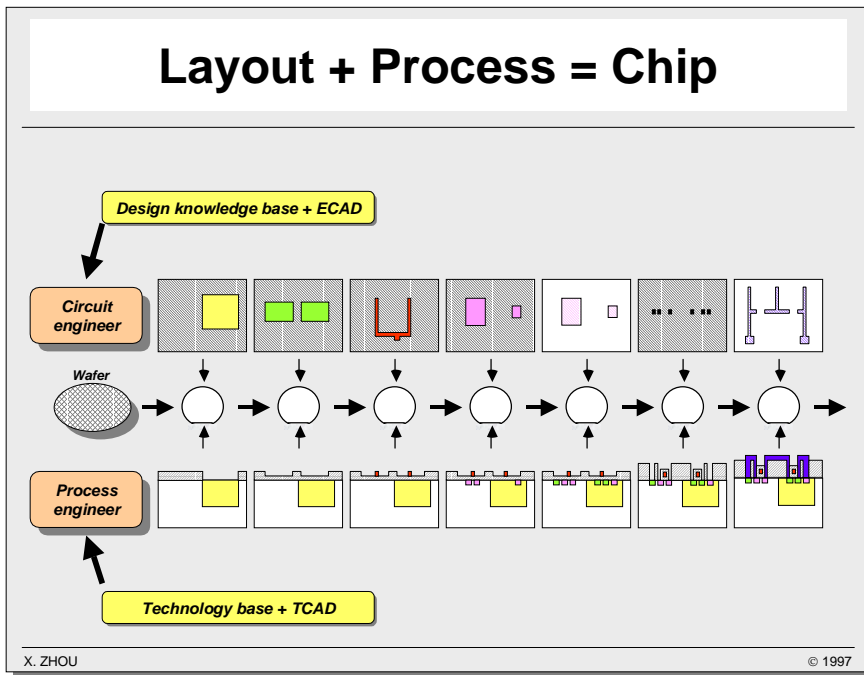
From another point of view, the final physical design (layout) of the system must be implemented into the silicon chip (or “committed to silicon”). This process involves the application of each individual mask during the processing of the silicon wafer. Again, take the inverter as an example, the final completion of the “device” consists of a sequence of processing steps, such as diffusion, oxidation, and ion implantation, for a given technology. The final performance of the system (the “device”) not only depends on the physical design (layout), but also on the process in which the device structures and doping profiles are altered. Imagine that for the whole system, this combination of layout and process must work “laterally” for all layers of the masks as well as “vertically” for all layers of depths.

New Technology Development

A new technology development is the process of achieving the optimum device performance through process variations. Generally, it involves three streams of knowledge: device physics, processing technology, and circuit design. It is centered at a specified process recipe since the final target is a process flow to implement the optimum design into the silicon chip. However, process variation must be constrained by the design rule and the scaling rule. The transistor electrical characteristics are closely coupled with the doping profiles and layer structures, and very often, trade-off must be taken for different design targets. Processing technology, such as the self-aligned technology, is also linked to the mask design and limited by photolithography.

Traditionally, technology development is relatively independent of the circuit design. However, when going into the deep-submicron regime, the conventional scaling rule does not apply any more. Device performance is closely coupled with the fabrication parameters and

circuit design constraints. Circuit designers also need process information (such as interconnect delays) at the very early stage of the design. Many of the conventional scaling rules and design methodologies are changed.



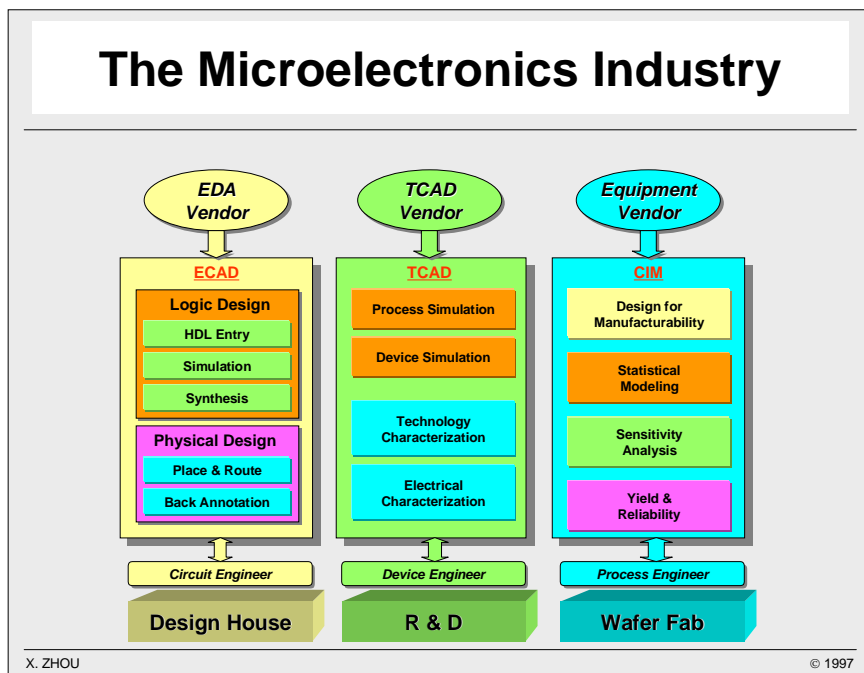
The Microelectronics Industry

Traditionally, the microelectronics industry consists of two major sectors: the *design house* where chips are being designed by system/circuit engineers, and the *wafer fab* where chips

are being fabricated by process/device engineers. In a design house, extensive electronic computer-aided design (ECAD) tools supported by the EDA vendors are used. A design session generally involves an iterative process from logic design (frontend) to physical design (backend). In a wafer fab, expensive equipment from the equipment vendors are used to fabricate the chips. The primary concerns are things like design for manufacturability, statistical modeling, sensitivity analysis, yield and reliability, all supported by computer integrated manufacturing (CIM).

The link between the design house and the wafer fab has been the mask information (GDS II files) and a set of SPICE parameters. The design house provides the mask information for the wafer fab, and the fab provides the SPICE parameters for the particular process to the design house. However, the SPICE parameters, which are needed in the circuit design, will not be available before the device is fabricated. For deep-submicron technologies, this information and, in particular, the interconnect delay information, is critical at the very early stage of a design (before fabrication).

With the rapid advancement of process and device models, technology computer-aided design (TCAD) tools are developed by the TCAD vendors to emulate wafer fabrication and device characterization. Realistic process information (layer thickness and doping profiles) can be obtained from process simulation, and electrical information (I–V and C–V characteristics) can be obtained from 2D device simulation. Then, SPICE parameters can be obtained through parameter extraction based on the simulated electrical characteristics, and delay information can be obtained through technology characterization. So far, the TCAD approach to technology development and transistor design has been widely used by all semiconductor companies, but it is mainly restricted to the device engineer and R&D community.



VIRTUAL WAFER FAB

One of the challenges of the deep-submicron technology is due to the fact that as transistor dimensions are getting smaller, their performance is more closely coupled with the fabrication parameters, and the interconnect delay is becoming dominant. This means that the transistor structure and processing information need to be considered in the early stage of a design before it is fabricated. This new trend places demands for new design methodologies as well as new design tools.

Chip Design and Wafer Fabrication

The semiconductor industry or, to a larger extent, the microelectronics industry, involves chip design and wafer fabrication, which is a complex, iterative process of “design – manufacturing – characterization – simulation – verification.”

A chip design starts with the product specification, followed by the frontend and backend designs. In this phase, ECAD tools have been developed so powerful that the logic design can be synthesized from a high-level hardware description language (HDL), the circuit netlist can be extracted from the logic functional description, and the layout can be extracted from the circuit- and logic-level descriptions.

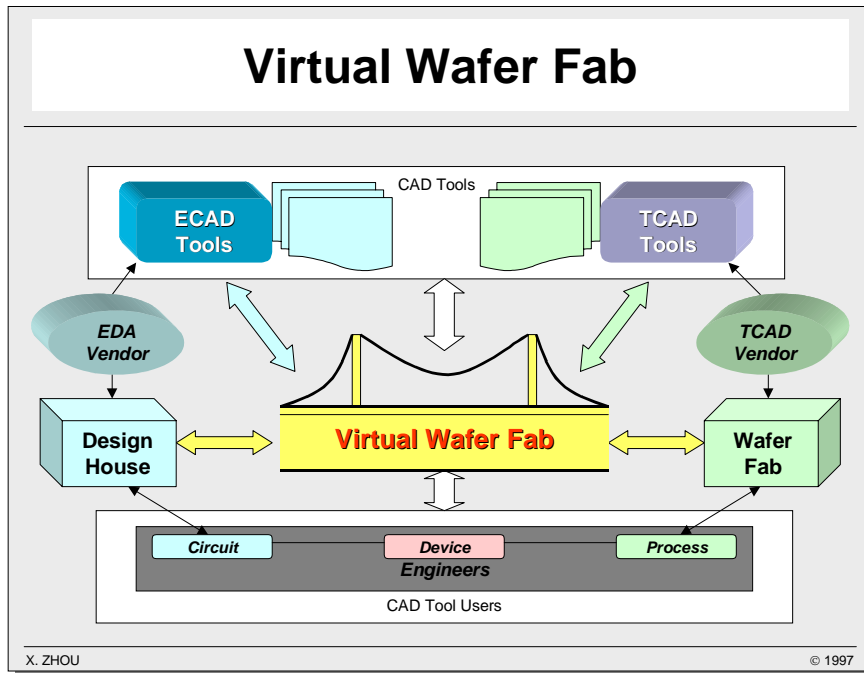
Once a set of mask has been designed, it is combined with a given process recipe in the manufacturing phase in a “real wafer fab” (RWF). Electrical and technological characterization is then performed on the fabricated device to extract the parameters for back-annotation and verification.

Although the EDA tools (including design and verification tools) are already quite advanced, this “design – manufacturing – characterization – verification” loop can be very costly if a “first-time silicon success” cannot be achieved. Moreover, it would be extremely expensive and time consuming if a new technology is to be developed using this iterative experimentation.

With the maturity of TCAD tools, real wafer fabrication can be emulated by process simulation, from which realistic device structures and doping profiles can be generated, and transistor performance can be characterized through device simulation with reasonable accuracy. Interconnect delays can also be extracted through technology characterization with 3D accuracy, which can provide information for design rule checker (DRC) and layout parasitic extraction (LPE) tools in the physical design. SPICE parameters can also be extracted from the “virtual device” I–V characteristics for back-annotating circuit simulators and timing analyzers, which provides the notion of “calibrating” ECAD tools based on TCAD tools. It is obvious that there is great incentive to develop this “virtual wafer fab” (VWF) technology to supplement the RWF experimentation.

Of course, how effective this approach will be in aiding first-time silicon success depends on how well the process and device simulators are calibrated to the RWF results. This calibration involves another loop — “manufacturing – calibration – simulation – verification.” The process models must be calibrated to the experimental doping and carrier

should not be “tweaking coefficients for all days.” It should be used for “testing concepts by analysis and design.”



Multi-Variable Design Space Multi-Target Optimization

Level	Variables	Targets
Circuit 	Spice: Model parameters, ... Geometrical: Channel length, width, ... Electrical: Supply voltage, substrate bias, ...	Digital: Delay, rise/fall time, drivability, off-state current, noise margin, ... Analog: Voltage gain, cutoff frequency, slew rate, gain-bandwidth, ...
Device 	Structural: Oxide thickness, junction depth, sheet resistance, ... Doping: Peak/surface concentration, ... Electrical: Supply voltage, substrate bias, ...	Electrical: Threshold, transconductance, subthreshold swing, saturation current, punchthrough current, junction capacitance, lifetime, ... Physical: Potential, field, charge, current, carriers, velocity, ...
Process 	Oxidation: Temperature, time, ambient, ... Implantation: Dose, energy, tilt, damage, ... Diffusion: Defect, stress, OED, TED, ...	Layer: Oxide thickness, junction depth, sheet resistance, ... Profile: Peak/surface concentration, projected range/straggle, ...

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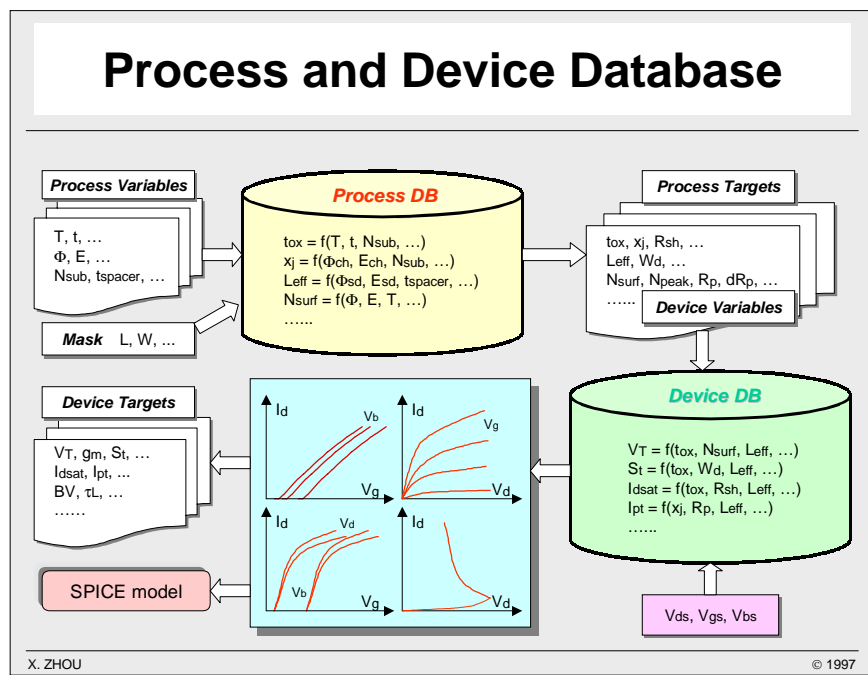
The multi-target optimization problem should be decomposed at different levels: process, device, and circuit. The target values of a specified gate delay, threshold voltage, or subthreshold swing, etc. depend on different variables at different levels. Transistor characteristics are more related to device parameters such as gate oxide thickness, junction depths, effective channel length, etc., which are indirectly related to processing variables such as oxidation time and temperature, implant dose and energy, etc. It is important to break

these dependencies at different levels so that they can be tackled more accurately and efficiently.

Process and Device Database

The first step is to identify target parameters to be designed or optimized. The specification will be different for different applications. For example, threshold voltage is one of the most important parameters in CMOS circuits, which is influenced by many variables. Any process variations, such as gate oxidation time or temperature, threshold adjustment implant dose or energy, will have direct impact on the final threshold voltage. However, from the device modeling point of view, it is the gate oxide thickness and the channel doping profile which influence the device electrical characteristics.

Hence, it is advantageous to construct separate databases for the processes and devices. For the process database, the input will be the processing variables and mask information, and the output will be the layer structures and doping profiles. The database stores all the input–output dependency data and, if possible, compact models linking the input and output can be developed. The device database, on the other hand, takes the device structure and biasing condition as input and stores the generated I–V characteristics, from which device targets can be extracted. Again, it would be extremely useful and efficient if compact analytic models at the device level can be developed based on the detailed TCAD results. Finally, circuit-level parameters and interconnect delays can also be extracted from the “virtual device” I–V characteristics.



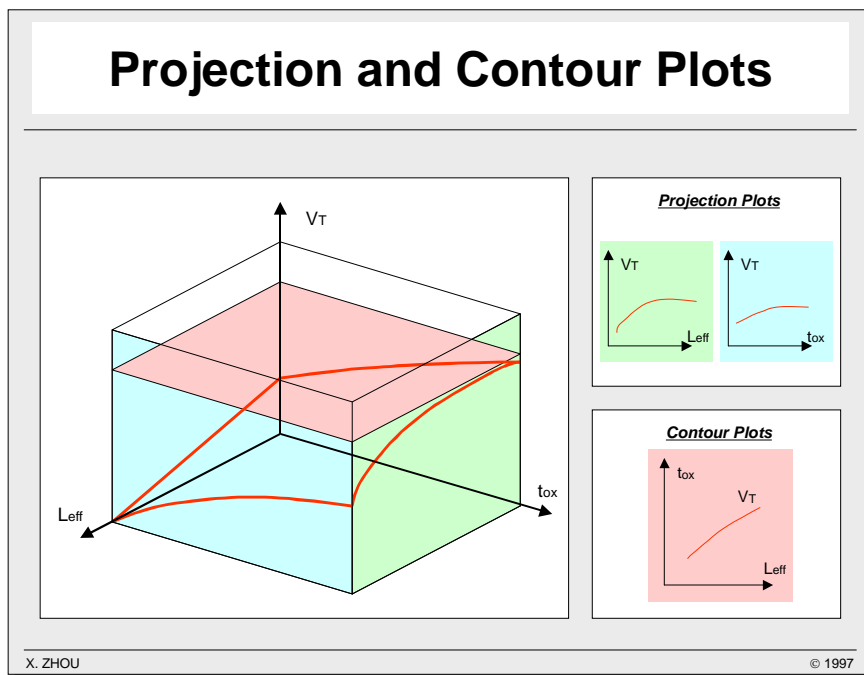
Projection and Contour Plots

Once a complete process and device database is constructed, a specified set of multi-target objects can be readily accessible from the multi-variable design space. These targets can be

visualized graphically by 3D plots, e.g., a plot of the threshold voltage (V_t) as a function of the effective channel length (L_{eff}) and the gate oxide thickness (t_{ox}).

These 3D data can be viewed in different ways at the designer's discretion. One type is the *projection plot* in which the target is plotted against one major variable, optionally with a secondary variable as a parameter. The other type is the *contour plot* in which constant values of the target are plotted against two major variables.

These plots can be generated directly from the database. If compact models are developed, it would be extremely efficient to generate these plots, which can be used for multi-target optimization.

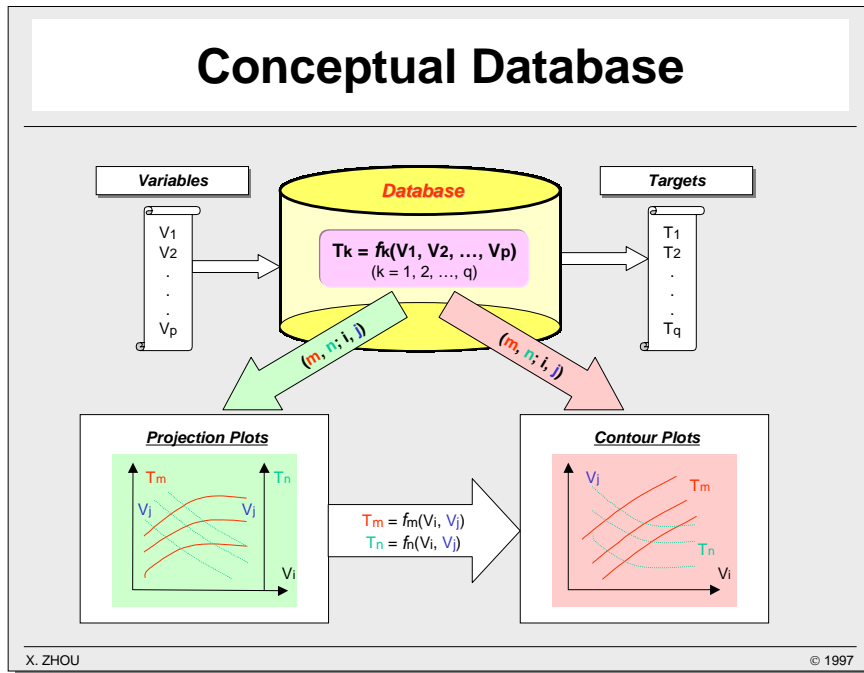


Conceptual Database

A conceptual database is described as one which stores the target–variable dependency data in a form easily accessible to the user. Each target in the database can be related to a number of variables. These data are generated from a complete set of simulations based on the TCAD models, which includes all the nonuniformities in chemical/electrical distributions and the nonlinearities of carrier transport. Each target–variable dependency represents a particular design of experiment (DOE). If a compact model is developed for a particular dependency, an analytic functional relation for that dependency is also defined.

Conceptually, data can be manipulated to obtain any view of a specified target. For example, projection plots of the m th target as a function of variable i for different values of variable j can be generated at the choice $(m; i, j)$, and the n th target can also be plotted in the same way for comparison. Likewise, by specifying the target values for the m th and n th targets, contour plots can be obtained as a function of two variables i and j . These plots and data can be used

for nonlinear regression, response surface modeling (RSM), and simultaneous optimization of multiple targets.



PROJECT DOUST

Project DOUST (Design and Optimization of Ultra-Small Transistors) is initiated with the express motivation of constructing a framework that segments the design and optimization of ultra-small transistors. The purpose of the conceptual framework is to provide an efficient and cost-effective aid to new technology development and transistor design and optimization.

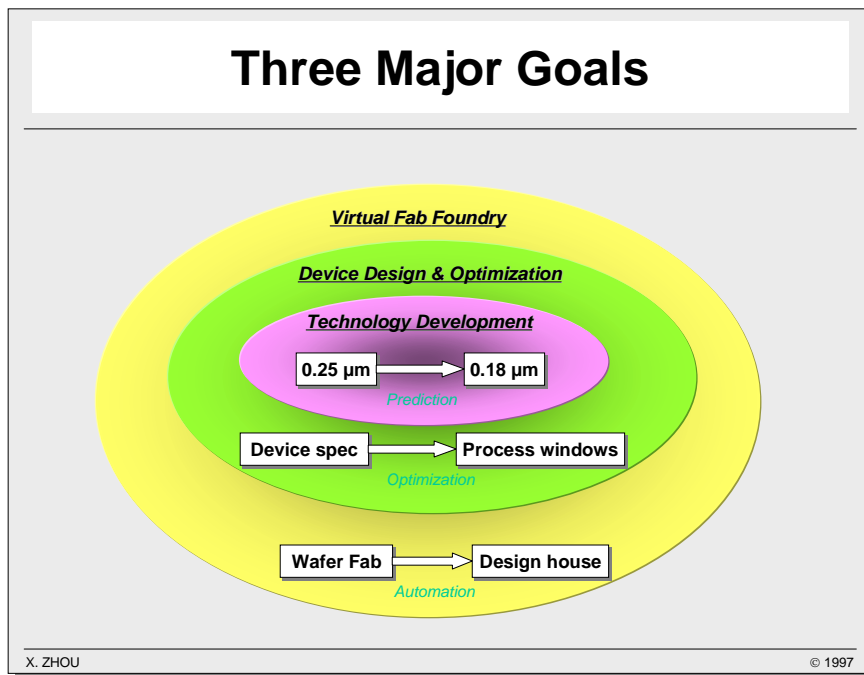
This project has started as a joint project between Nanyang Technological University (NTU) and Chartered Semiconductor Manufacturing Ltd. (CSM) in the context of the 0.18- μm CMOS process technology to be developed by CSM.

Three Major Goals

There are three major goals for Project DOUST. For immediate interests, it is aimed at predicting the 0.18- μm technology to be developed based on a TCAD-calibrated VWF technology from an existing 0.25- μm technology. To a larger extent, a framework will be constructed to aid ultra-small transistor design and optimization by providing "process windows" for a given set of device performance specifications. Ultimately, this project will be a first step towards the establishment of a "virtual fab foundry" (VFF) to bridge the gap between the wafer fab and the design house.

Specific objectives as set out by the joint project are listed below:

1. Construct a framework for the TCAD approach to new technology development and transistor design and optimization.
2. Calibrate process and device simulators based on an existing process (0.25 μm) so that the developed models can be used in new processes (0.18 μm), which are to be verified with experimental devices.
3. Determine process windows for the given device performance targets through Design of Experiments (DOE) to bracket the final optimal design.
4. Formulate simplified analytic/empirical equations based on the full TCAD simulation to give a first-order approximation on the device performance in relation to process variables.
5. Extract circuit parameters from “virtual wafer” experiments, from which a complete TCAD environment will be established.
6. Investigate specific process and device phenomena through advanced physical modeling and simulation.
7. Provide a training ground for professional scientists and engineers in semiconductor processes and devices.

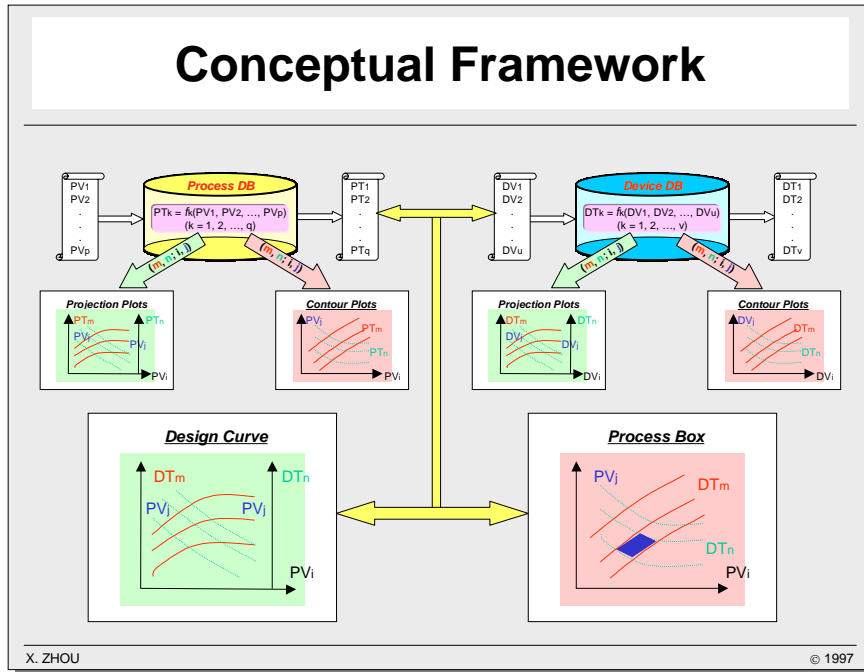


Conceptual Framework

The conceptual framework is based on the process database and the device database constructed from the TCAD simulations. Suppose, for example, there are q process targets, each one is a function of one or more of the p process variables; and there are v device targets, each one is a function of one or more of the u device variables. In many cases, a process target is also a device variable (e.g., t_{ox} , L_{eff} , x_j).

The conceptual framework will be able to link the device targets to the process variables. This means that two types of information (plots) can be obtained: (1) *Design curve* in which one or more device targets can be plotted against one major process variable and, optionally,

with a secondary process variable as a parameter for comparison. (2) *Process box* in which contours of one or more device targets can be plotted against two major process variables. The design curves and the process boxes can be very useful in aiding technology development and multi-target transistor optimization.



Methodology of Implementation

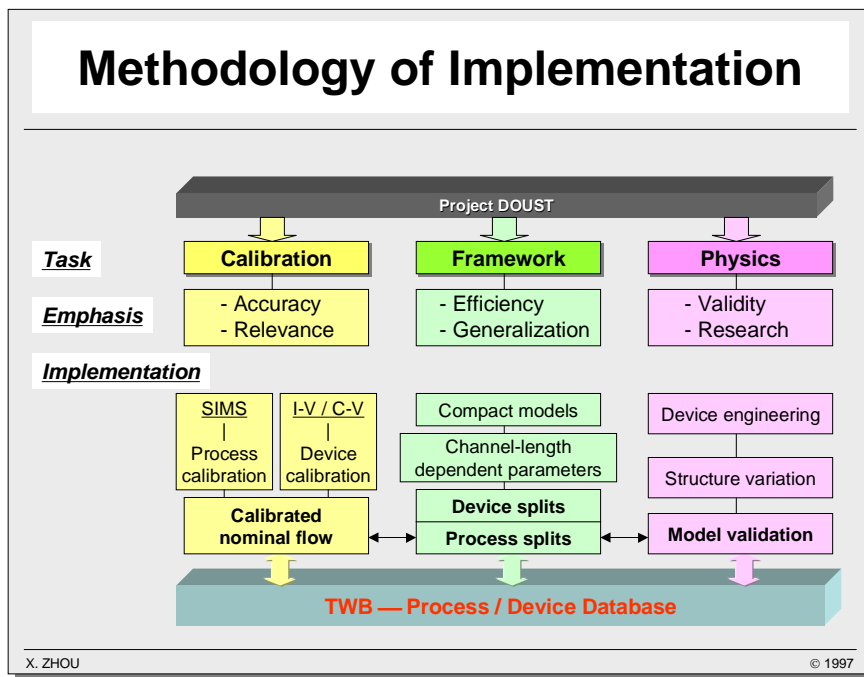
Project DOUST is to be implemented with three tasks in parallel: calibration, framework, and physics, with different emphasis for each task.

Calibration work aims at the accuracy of the simulator models and the relevance of the simulation results. Physics study mainly concerns with the validity of the process/device models being used, since we are pushing to the limit of our current understanding. For the framework design, however, the focus is mainly on the efficiency and generalization. Of course, the usefulness of the developed framework depends on how well we calibrate the models (accuracy) and how well we understand the device physics (validity).

Implementation of the above three tasks can be carried out in parallel, with close interaction among them. Everything will be based on the 0.25- μm CMOS process being developed at CSM. Process simulator will be calibrated to the SIMS measurements, and device simulator will be calibrated to the measured I-V and C-V characteristics. An up-to-date calibrated nominal flow will be made available for other tasks. Device-model validation will be studied with different structures and biasing conditions, and the results will be fed back to the other two modules. Research on device engineering (e.g., channel doping and drain engineering) will also be conducted. A framework will be constructed by running extensive process and device splits to build the process and device databases. Channel-length dependent parameters will be extracted from the database to provide a guide for technology scaling. Compact models for the target-variable dependencies will be developed. The information will be

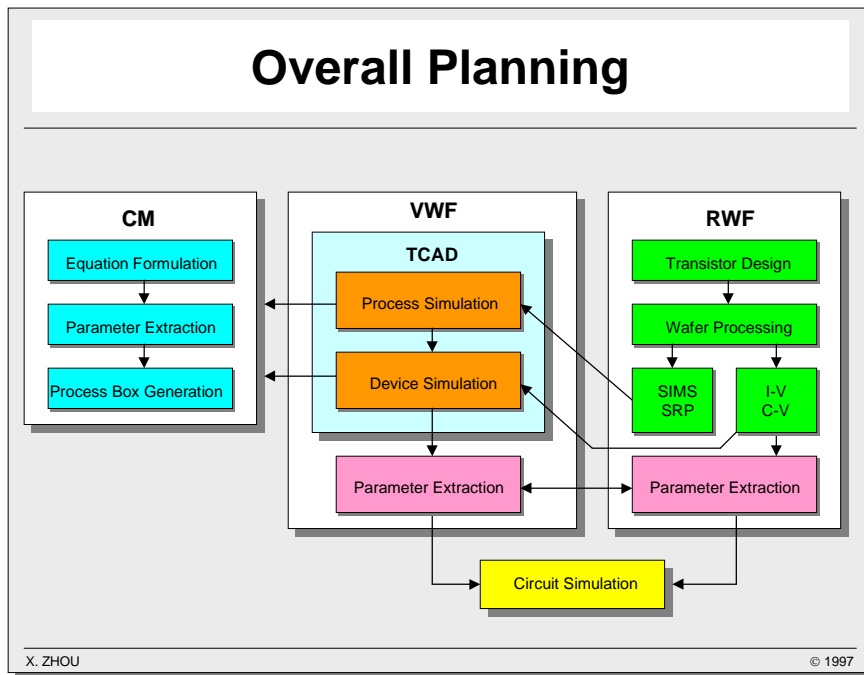
shared among the three modules through the process/device database under the TMA WorkBench (TWB).

Eventually, given a more accurately calibrated model, or a new process recipe, the framework should be able to generate a new database, the process windows to bracket the final optimum design, and the compact models as an efficient design guide, all within the region of validity of the models used.



Overall Planning

There are three major modules in the overall planning for Project DOUST: *Virtual Wafer Fab* (VWF), *Real Wafer Fab* (RWF), and *Compact Modeling* (CM). It is centered at the core TCAD environment — process and device simulations. The VWF module forms a self-contained system, from process specification to circuit parameter extraction, which is in parallel with the RWF module. Comparison of circuit performance between the VWF and RWF modules can be made at the transistor level or at the circuit level through SPICE circuit simulation. The RWF module provides experimental data to be used in process/device simulator calibration as well as verification of the developed technology and the compact model. The CM module depends on the TCAD results, and it provides a first attempt at formulating higher-level modeling of process–device–circuit inter-dependencies from a lower-level model.

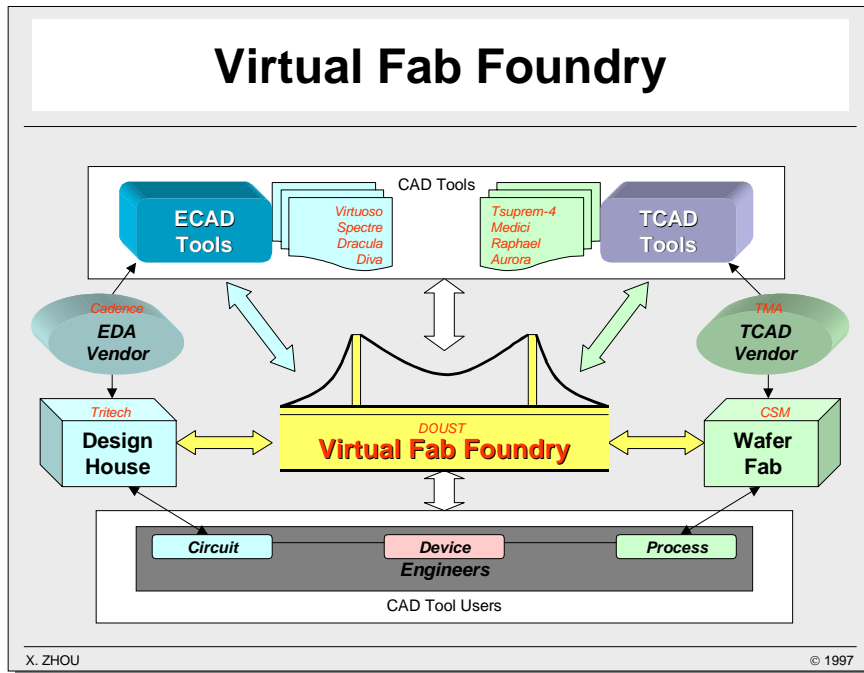


Virtual Fab Foundry

When we look at the current status of the EDA industry as well as the chip design and fabrication practice, three trends can be observed. First, design house and wafer fab are relatively independent of each other, but there is an increasing need for coupling and information exchange between the two. Secondly, most existing ECAD tools do not take into consideration of the real (gate and interconnect) delay information from the actual transistor structure and layout, and it is increasingly important to consider these effects at the early stage of a design. Finally, although the TCAD approach to transistor design and technology development is becoming popular, it is mainly restricted to R&D groups and semiconductor companies, and there is a barrier for the general CAD tool users since use of these TCAD tools requires advanced knowledge of process and device physics. In fact, TCAD vendors are already beginning to provide professional services to customers for calibration and efficient use of their tools.

The idea of the “virtual fab foundry” is to bridge the gap between the design house and wafer fab, to link ECAD tools with TCAD information, and to provide services to the CAD tool users. Project DOUST is a first step towards the establishment of such a foundry. Take the local design house, Tritech, and the wafer fab, CSM, as an example. Suppose a Tritech’s design is to be fabricated by CSM. Based on the robust database the virtual fab foundry has implemented and calibrated to the CSM’s technology, a set of SPICE and interconnect delay parameters could be generated and provided to Tritech even before the design is fabricated. Even designs using new technologies, which have not been developed, can be predicted. Other important information, such as statistical SPICE parameters due to process variations, can also be generated from the virtual fab foundry.

Ultimately, successful implementation of the VWF technology could lead to the general services to the chip design and fabrication industry with the idea of internet-based TCAD.

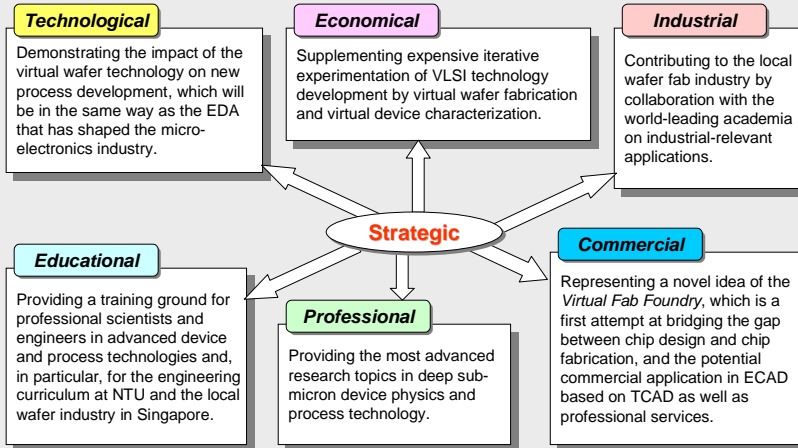


Summary: Strategic Factors

In summary, the proposed Project DOUST has the following strategic factors:

1. **Technological:** It demonstrates the impact of the virtual wafer fab technology on new process development, which will be in the same way as the EDA that has shaped the microelectronics industry.
2. **Economical:** It supplements expensive iterative experimentation of VLSI technology development by virtual wafer fabrication and virtual device characterization.
3. **Industrial:** It contributes to the local wafer fab industry by collaboration with the world-leading academia on industrial-relevant applications.
4. **Educational:** It provides a training ground for professional scientists and engineers in advanced device and process technologies and, in particular, for the engineering curriculum at NTU and the local wafer industry in Singapore.
5. **Professional:** It provides the most advanced research topics in deep-submicron device physics and process technology.
6. **Commercial:** It represents a novel idea of the *Virtual Fab Foundry*, which is a first attempt at bridging the gap between chip design and chip fabrication, and it has potential commercial applications in ECAD based on TCAD as well as professional services.

Summary: Strategic Factors



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