

EE4613 Course Schedule (Device/Integration Modules)

EE4613

CMOS Process and Device Simulation

No.	Week of	Subject	F61	F62
			Monday	Thursday
			8:30–11:30	1:30–4:30
5	7 Sep	Introduction: Device Modeling	7/9	19/9
6	14 Sep	VDS: Device Simulation	14/9	17/9
7	21 Sep	VDS: Design Exercise	21/9 → 22/9@1:30pm	24/9
B	28 Sep	TWB: WorkBench DOE	28/9	1/10
8	5 Oct	VPI: Process Integration	5/10	8/10
9	12 Oct	Break (swap)	Break	Break
10	19 Oct	VPI: Design Exercise	19/10 → 20/10@1:30pm	22/10
11	26 Oct	VPI: Design Exercise	26/10	29/10
12	2 Nov	VPI: Design Exercise	2/11	5/11
13	9 Nov	Design Exercise / Summary	9/11	12/11

Venue: Nanoelectronics Design Lab (S2-B5b-05)

Continuous assessment:

- **Design Exercise report** (per subgroup). See *Notes* in the Design Exercise.
Due: **16 Nov 2009**. Submit to NED Lab; collect before exam.
- **Individual performance** (based on lab participation and activities, including Q&A).

Final examination: Two hours. Open book, open notes, open mind. Covers the full contents (3 Modules).