

The Missing Link to Seamless Simulation

Multilevel modeling of nanometer CMOS ULSI systems based on a compact model and single-engine simulator

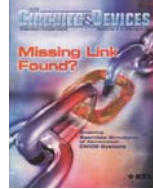
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Technological Thrust

In the 2001 edition of *International Technology Roadmap for Semiconductors (ITRS)*:



“*Seamless integration of simulation modules*” is considered as one of the difficult challenges beyond 2007, with an example of “*a complete simulation chain linking process modeling, device modeling, compact model extraction, and library generation.*” In the 2002 update of ITRS, “*compact modeling including more physical models and statistics*” has been added to the modeling needs beyond 2007, which also “*changes the Grand Challenges for the ITRS.*”



Invited feature article of the cover story:
IEEE Circuits & Devices Magazine
Xing Zhou
(Vol. 19, No. 3, pp. 9–17, May 2003)



Call-outs from the feature article:

- The quality of the models and tools determines not only whether the design works or not, but also how well it works for the same technology.
- The real challenge is how to “propagate” the detailed physics captured in a lower-level (process/atomic) model to higher-level (circuit/block) abstractions.
- From the model/tool development point of view, the challenge is to build a consistent modeling infrastructure from process through device/circuit to systems.
- The key to having a consistent multilevel solution is to have a dual representation at each level.
- There is a missing link between the model developers and circuit-simulator vendors as well as between the technology developers and circuit designers.

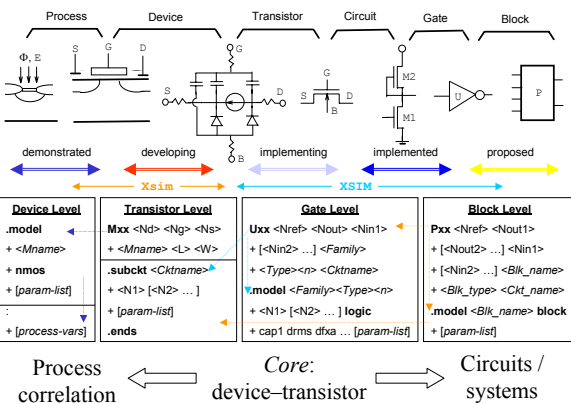
Breakthrough Principle & Benchmarking

Key features of Xsim compact model

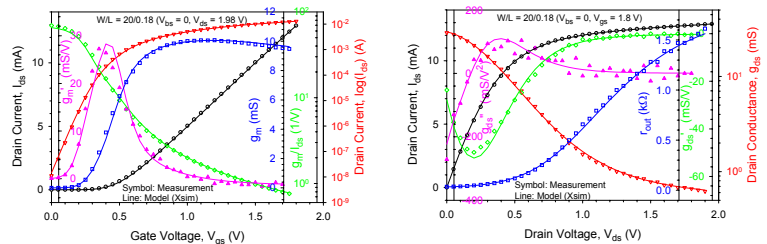
- Unified regional threshold-voltage-based consistent DC/AC model
- Symmetrical, continuous, and scalable/predictive in geometry/bias
- Non-binnable technology characterization with one-iteration parameter extraction using minimum measurement data

Key features of XSIM mixed-mode simulator

- Dual digital/analog representation with internal subcircuit expansion
- Implicit/automatic circuit partition and dynamic mode switching
- Dynamic-delay calculation

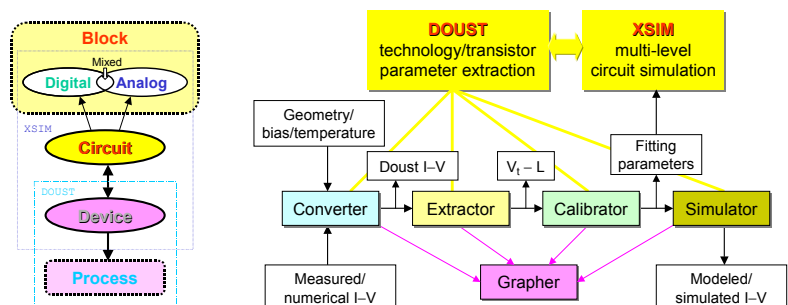


0.18-μm technology characterization and modeling



Gate characteristics & higher-order derivatives

Drain characteristics & higher-order derivatives



DOUST: Design and Optimization of Ultra-Small Transistors

Website: <http://www.ntu.edu.sg/home/exzhou/Research/DOUST/>

Commercial Impact & Interested Parties

Technology-Based Predictive Compact Model Development for Next Generation CMOS

Funded by Semiconductor Research Corporation® through a Research Customization Program (RCP) supported by Chartered Semiconductor Manufacturing



Primary goal: A unified compact model for next generation CMOS circuit simulation that is accurate, continuous, symmetric, and scalable for a given (deep-submicron/nanometer) technology, with minimum parameter set and easy extraction, and with predictive capability for the N+1 (and N+2) technology nodes.

Supports and Collaborations

- Nanyang Technological University, Singapore
- Chartered Semiconductor Manufacturing, Singapore
- LSI Logic Corp., USA
- Institute of Microelectronics, A*STAR, Singapore
- Stanford University, USA
- Institute of Microelectronics, Tsinghua University, PRC
- Indian Institute of Technology – Bombay, India
- Hiroshima University, Japan

Next Generation CMOS Modeling

- “Everything should be made as simple as possible, but not any simpler.” (Albert Einstein)
- “The best way to predict future is to invent it.” (Alan Kay)