

Unified Approach to MOS Transistor Compact Modeling

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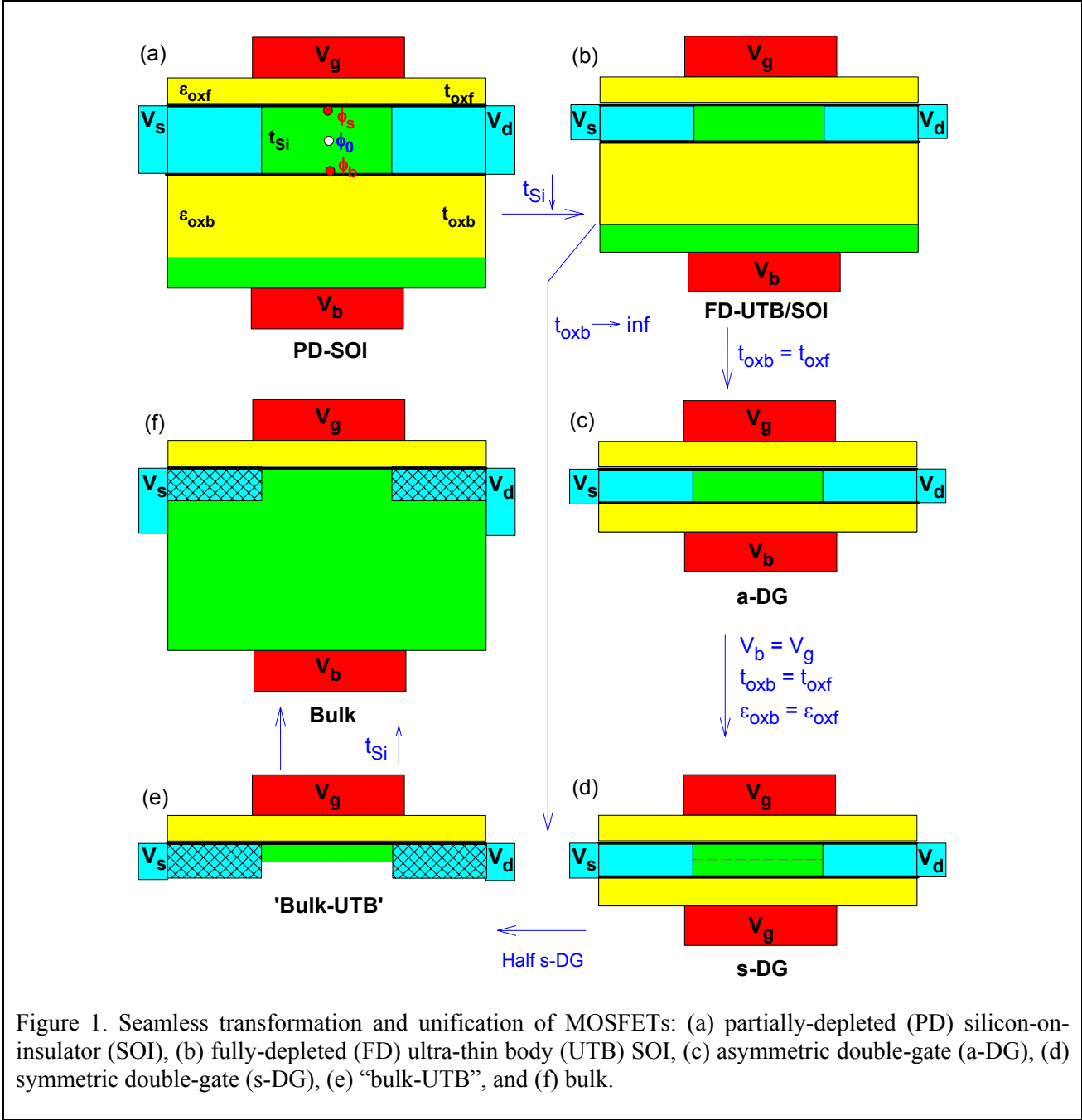


Figure 1. Seamless transformation and unification of MOSFETs: (a) partially-depleted (PD) silicon-on-insulator (SOI), (b) fully-depleted (FD) ultra-thin body (UTB) SOI, (c) asymmetric double-gate (a-DG), (d) symmetric double-gate (s-DG), (e) “bulk-UTB”, and (f) bulk.

Keywords: Compact model (CM), charge-sheet model (CSM), inversion-charge model (ICM), surface-potential model (SPM), threshold-voltage model (TVM), unified regional model (URM), MOSFET.

ABSTRACT

MOSFETs have been the building blocks of modern VLSI for decades. As classical bulk-CMOS scaling is approaching its physical limit, various types of non-classical CMOS emerge. Although different in structure, topology, and operation, different types of MOS transistors essentially function in a similar way governed by the same physical principles, and they are related one another as illustrated in Fig. 1. Accompanied with technology advancement, MOS compact models (CM) that are used in circuit simulators for designing integrated circuits have gone through many generations of development. Learning from past experience, it is important to construct a core model that is extendable to future technologies and devices rather than always “chasing” the technology. A careful examination of the fundamental physical equations governing various types of devices and operations is therefore necessary in order to come up with an approach to unifying various models into one framework.

In this paper, we review the basic voltage equations for the generic MOS transistor. We extend our unified regional modeling (URM) approach to bulk-MOS charge modeling with non-pinned surface potential for various device structures, such as partially-depleted (PD) or fully-depleted (FD) ultra-thin body (UTB) silicon-on-insulator (SOI) as well as symmetric/asymmetric double-gate (s-DG/a-DG) MOSFETs. The regional solutions make it easy to handle different device structures with explicit asymptotically physical solutions, and the unified solution combines the best features in different modeling approaches, such as surface-potential/inversion-charge/threshold-voltage based models, without the need to solve exactly at flat-band voltage. We show that it is viable to obtain a unified solution scalable with layer thickness and doping in all bias ranges (accumulation, depletion, weak/volume/strong inversions). In particular, the effect of doping (even unintentional) in DG MOSFETs is studied with the regional approach. The ultimate goal is to have one generic and scalable model with selectable accuracy and seamless transition across device types and operations.

INTRODUCTION

The most *complete* MOSFET model for the implicit (input) voltage equation [1] and double-integral (output) current [2], and the *simplest* drift-current model [3] based on fixed bulk-charge and pinned surface-potential were both proposed by Sah 40+ years ago; the former still serves as the “golden reference” for benchmarking bulk-MOS compact models and the latter is taught in all elementary MOSFET theory. For an “ideal” long-channel uniformly-doped MOSFET, either model can be used for

describing terminal characteristics (the simple model is preferred for device/circuit analyses); whereas for a nanoscale MOSFET, neither model is sufficient to be used without taking into account various short-channel/narrow-width/high-field/quantum effects. The history of MOS transistor CM development [4], since the introduction of the charge-sheet model (CSM) [5], has followed the “simple” threshold-voltage (V_t) modeling (TVM) formalism for three decades, not because of people not being aware of the “complete” physical description by the surface potential (ϕ_s) but mainly due to not having such high accuracy demand offered by the surface-potential models (SPM) in the early days for digital designs. Inversion-charge (Q_i) modeling (ICM) approaches seek to overcome some major obstacles in V_t -based models (such as symmetry and continuity) through a linearization of Q_i with respect to ϕ_s ; whereas ϕ_s -based formulations describe the terminal charges/currents in terms of ϕ_s , which is solved iteratively or explicitly from the (input) voltage equation.

High accuracy demands drive the development of more accurate description of surface potentials and charges [6]. Although it is known that accurate iterative ϕ_s solutions for bulk-MOS are readily available, the question is: will the iterative (whether by numerical or analytical) ϕ_s -based formalism be the best core model for future generations of various types of MOS devices?

As bulk-CMOS scaling is driven to its limit, various non-classical devices emerge, such as ultra-thin body (UTB) and silicon-on-insulator (SOI) MOSFETs. For SOI MOSFETs, the fundamental input voltage equation will be modified due to the change in the bottom boundary condition. Depending on the channel thickness and doping, the SOI MOSFET may work in partially-depleted (PD) or fully-depleted (FD) mode. Another scalable parameter would be the bottom oxide thickness which, if comparable to the gate oxide thickness, results in asymmetric double-gate (a-DG) operation; or a symmetric-DG (s-DG) device when the top and bottom oxides and the front- and back-gate biases become the same, such as in a FinFET. Although these different types or operations of devices have distinct technologies and topologies as well as applications, transitions from one type to another should really be *seamless* (from a theoretical point of view) when physical layer thickness as well as doping and bias are varied. Now, the question is: do we want different core models for different types of devices, or one unified model that can handle all device types and operations? The real question (or challenge) is ***the right choice of model infrastructure*** that is extendable and flexible such that, when non-classical alternative devices emerge in real applications, the model under development will be ready with seamless transitions from “bulk-like” to “DG-like” structures. Figure 2 illustrates the history and future trend of MOS transistor compact models.

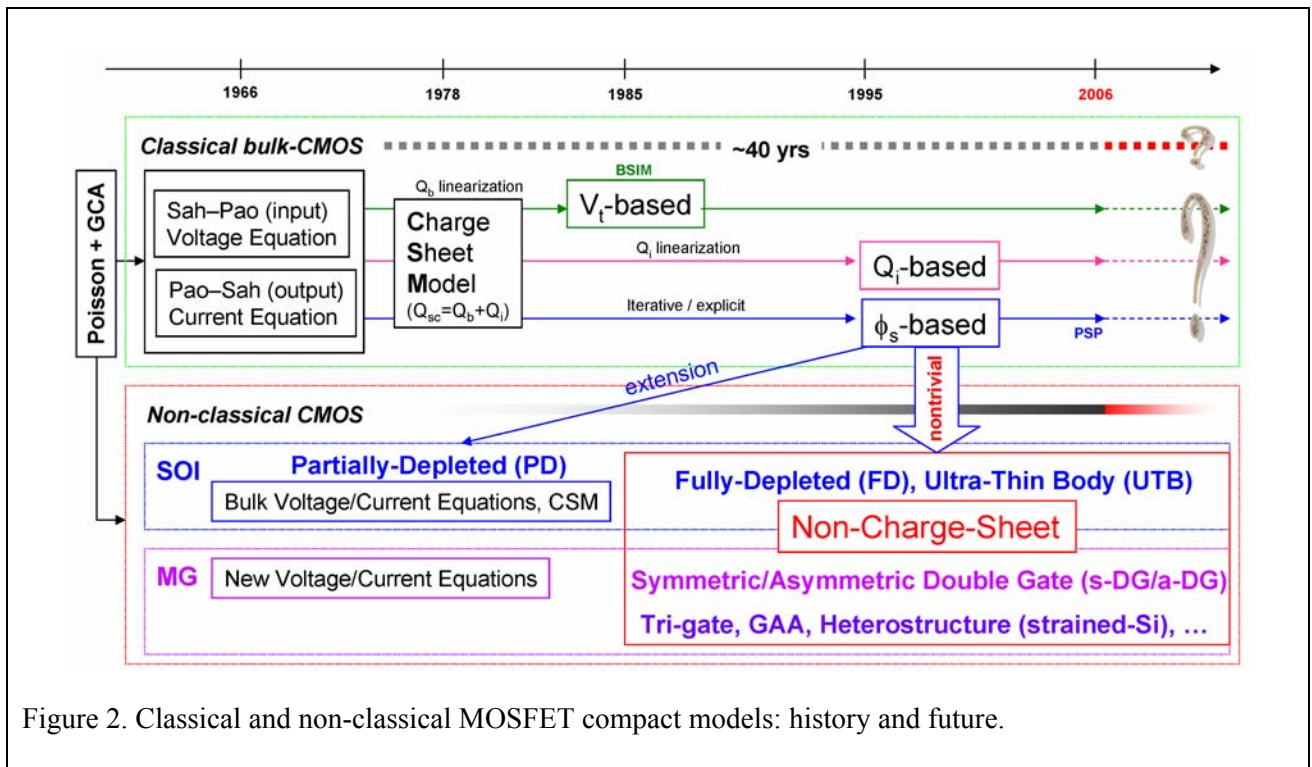


Figure 2. Classical and non-classical MOSFET compact models: history and future.

It can be very challenging (if not impossible) to handle all these device types within the same iterative/explicit ϕ_s -based core model, since it is known the solution to the voltage equation is non-integrable for *doped* s-DG/a-DG devices. This may be the reason why existing literature on DG models all assumes *undoped* channel. However, a model developed with “undoped” assumption cannot be extended to doped devices; nor can it accurately model real devices in which unintentional doping is always present. On the contrary, a model developed with doping scalability, although much more difficult, contains undoped devices. The motivation in extending our URM approach to surface-potential and charge modeling for bulk-CMOS [7] to SOI/DG MOSFET modeling is an attempt to unify various types of devices with different governing equations.

UNIFICATION OF MOS MODELS

The Master (Input) Voltage Equation

Using *n*MOS as the example and following the coordinate in the generic MOSFET structure shown in Fig. 3, and under the gradual-channel approximation (GCA): $d^2\psi/dy^2 \ll d^2\psi/dx^2$, the Poisson equation is written as

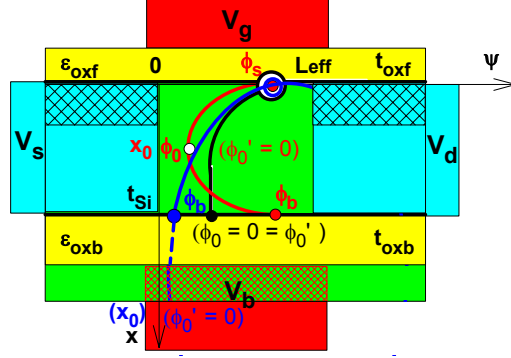


Figure 3. Generic MOSFET structure and schematic potential distributions for three cases.

$$\begin{aligned}
 \frac{d^2\psi}{dx^2} &= -\frac{\rho}{\epsilon_{Si}} = -\frac{q(p-n+N_D-N_A)}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}}(n-p+N_A-N_D) \\
 &= \frac{q}{\epsilon_{Si}} \left[n_i e^{(\psi-\phi_F-V_c)/v_{th}} - n_i e^{-(\psi-\phi_F)/v_{th}} + n_i e^{\phi_F/v_{th}} - n_i e^{-(\phi_F+V_c)/v_{th}} \right] \\
 &= \frac{qN_A}{\epsilon_{Si}} \left[e^{(\psi-2\phi_F-V_c)/v_{th}} - e^{-\psi/v_{th}} + 1 - e^{-(2\phi_F+V_c)/v_{th}} \right] \\
 &\equiv \frac{qN_A}{\epsilon_{Si}} G(\psi, V_c).
 \end{aligned} \tag{1}$$

Based on $E_x = -d\psi/dx$, using the following transformation

$$\frac{d^2\psi}{dx^2} = -\frac{dE_x}{dx} = -\frac{dE_x}{d\psi} \frac{d\psi}{dx} = E_x \frac{dE_x}{d\psi}$$

and the “generic” boundary conditions (at $x = 0$ and $x = x_0$)

$$\psi(0, y) = \phi_s(y), \quad E_x(0, y) = E_s(y) = -\phi'_s(y) \tag{2a}$$

$$\psi(x_0, y) = \phi_0(y), \quad E_x(x_0, y) = E_0(y) = -\phi'_0(y), \tag{2b}$$

(1) can be integrated out as

$$\begin{aligned}
 \frac{E_s^2 - E_0^2}{2} &= \int_{E_0}^{E_s} E_x dE_x = \int_{\phi_0}^{\phi_s} \frac{d^2\psi}{dx^2} d\psi \\
 &= \frac{qN_A}{\epsilon_{Si}} \int_{\phi_0}^{\phi_s} G(\psi, V_c) d\psi \\
 &= \frac{qN_A}{\epsilon_{Si}} \left\{ e^{-(2\phi_F+V_c)/v_{th}} \left[v_{th} (e^{\phi_s/v_{th}} - e^{\phi_0/v_{th}}) - (\phi_s - \phi_0) \right] + v_{th} (e^{-\phi_s/v_{th}} - e^{-\phi_0/v_{th}}) + (\phi_s - \phi_0) \right\} \\
 &\equiv \frac{qN_A}{\epsilon_{Si}} F_s^2(\phi_s, \phi_0, V_c).
 \end{aligned} \tag{3}$$

The general boundary conditions are given for SOI/DG using the Gauss law at the front/top gate ($x = 0$):

$$E_s = -\phi'_s = + \frac{\varepsilon_{oxf} V_{gf} - \phi_s}{\varepsilon_{Si} t_{oxf}}, \quad (V_{gf} \equiv V_g - V_{FBf}) \quad (4a)$$

and the back/bottom gate ($x = x_0 = t_{Si}$; $E_0 = E_b$, $\phi_0 = \phi_b$):

$$E_0 = E_b = -\phi'_b = - \frac{\varepsilon_{oxb} V_{bf} - \phi_b}{\varepsilon_{Si} t_{oxb}}, \quad (V_{bf} \equiv V_b - V_{FBb}) \quad (4b)$$

where V_g and V_b are the front- and back-gate voltages, $V_{FBj} = \phi_{MSj} - Q_{oxj}/C_{oxj}$ and $C_{oxj} = \varepsilon_{oxj}/t_{oxj}$ are the flat-band voltage and oxide capacitance (per unit area), with ε_{oxj} and t_{oxj} being the oxide permittivity and thickness, respectively, for the front and back gate ($j = f, b$). Applying (4) to (3), one obtains *one* generic master (input) voltage equation with *two* unknowns (ϕ_s and ϕ_b), which can only be solved (conceptually) after assuming another relationship between them, since the second double-integral equation cannot be solved if doping is considered, which is given by the most generic expression below:

$$\frac{E_s^2 - E_x^2(x)}{2} = \frac{qN_A}{\varepsilon_{Si}} F_s^2 \{ \phi_s, \phi(x), V_c \} \quad (5a)$$

$$-\frac{d\psi}{dx} = E_x(x) = \left[E_s^2 - \frac{2qN_A}{\varepsilon_{Si}} F_s^2 \{ \phi_s, \phi(x), V_c \} \right]^{1/2} \equiv H \{ \phi_s, \phi(x), V_c \} \quad (5b)$$

$$-\int_{\phi_s}^{\phi_b} d\psi = \int_0^{x_0} H \{ \phi_s, \phi(x), V_c \} dx \quad (5c)$$

$$\begin{aligned} \phi_s &= \phi_b + \int_0^{t_{Si}} H \{ \phi_s, \phi(x), V_c \} dx \\ &= \phi_b + \int_0^{t_{Si}} \left[E_s^2 - \frac{2qN_A}{\varepsilon_{Si}} \int_{\phi(x)}^{\phi_s} G(\psi, V_c) d\psi \right]^{1/2} dx. \end{aligned} \quad (5)$$

This is the most generic case for a-DG MOSFETs, which is also the most difficult one to solve when doping is considered. When doping is not considered, (5) is integrable, which gives the second equation relating ϕ_s and ϕ_b .

The (Input) Voltage Equation with $\phi'_0 = 0$

Asymmetry in DG arises whenever the two gate's V_{FBj} , t_{oxj} , ε_{oxj} ($j = f, b$), as well as V_g and V_b are different. For symmetric DG with identical gate materials, oxide thickness, and $V_g = V_b$, the potential gradient at the mid-gap ($x_0 = t_{Si}/2$) is always zero ($E_0 = -\phi'_0 = 0$). This is also similar to the bulk-UTB with $\phi'_0 = 0$ at $x_0 = t_{Si}$, which is equivalent to one half of the s-DG. For FD-SOI when the bottom oxide

thickness $t_{oxb} \rightarrow \infty$, from the boundary condition (4b), $E_b = -\phi'_b \approx 0$. Under these conditions, (3) can be simplified to the following normalized surface field:

$$\begin{aligned} F_s(\varphi_s, \varphi_0, v_c) &\equiv \left[\int_{\phi_0}^{\phi_s} G(\psi, V_c) d\psi \right]^{1/2} = \frac{E_s}{\sqrt{2qN_A/\epsilon_{Si}}} \\ &= \text{sgn}(\varphi_s) \sqrt{v_{th} \left\{ e^{-(2\varphi_F + v_c)} \left[(e^{\varphi_s} - e^{\varphi_0}) - (\varphi_s - \varphi_0) \right] + (e^{-\varphi_s} - e^{-\varphi_0}) + (\varphi_s - \varphi_0) \right\}} \\ &\equiv \text{sgn}(\varphi_s) \sqrt{f_\phi(\varphi_s, \varphi_0, v_c)} \end{aligned} \quad (6)$$

in which $\varphi_s = \phi_s/v_{th}$, $\varphi_0 = \phi_0/v_{th}$, and $v_c = V_c/v_{th}$ are the normalized (to the thermal voltage, v_{th}) surface potential, potential at $x = x_0$, and channel voltage, respectively. Applying the boundary condition (4a) to (6), it gives *one* (input) voltage equation for the (front) gate:

$$V_{gf} - \phi_s = \text{sgn}(\phi_s) \gamma \sqrt{f_\phi(\phi_s, \phi_0, V_c)} \quad (7)$$

for the (coupled) ϕ_s and ϕ_0 solutions, in which $\gamma = (2q\epsilon_{Si}N_A)^{1/2}/C_{ox}$ is the body factor, and

$$\begin{aligned} f_\phi &\equiv f_\phi/v_{th} \\ &= \underbrace{e^{-(2\varphi_F + v_c)} \left[(e^{\varphi_s} - e^{\varphi_0}) - (\varphi_s - \varphi_0) \right]}_{(n)} + \underbrace{(e^{-\varphi_s} - e^{-\varphi_0})}_{(p)} + \underbrace{(\varphi_s - \varphi_0)}_{(N_A)}. \end{aligned} \quad (7a)$$

However, the second boundary condition (4b) cannot be written at $x = x_0$ since there is no Gauss law to be applied at that “boundary.” Again, another relationship between ϕ_s and ϕ_0 has to be found or assumed in order to solve the voltage equation (7) with $\phi'_0 = 0$ for s-DG/bulk-UTB MOSFETs. It is also clear to see that (7) is not integrable if doping (N_A term) is considered. However, regional solutions can be derived for the doped s-DG MOSFETs [8].

The Bulk-MOS (Input) Voltage Equation

It can be observed that when $\phi_0 = 0$ in (7), which is equivalent to bulk-MOS (and approximately PD-SOI) boundary condition, it reduces to the conventional bulk-MOS “Pao–Sah” voltage equation [1, 2, 4]:

$$\begin{aligned} V_{gb} - V_{FB} - \phi_s &= \text{sgn}(\phi_s) \gamma \sqrt{f_\phi} \\ f_\phi &= v_{th} \left\{ \underbrace{e^{-(2\varphi_F + v_{cb})} \left[(e^{\varphi_s} - 1) - \underbrace{\varphi_s}_{(N_D)} \right]}_{(n)} + \underbrace{(e^{-\varphi_s} - 1)}_{(p)} + \underbrace{\varphi_s}_{(N_A)} \right\}. \end{aligned} \quad (8)$$

It is noted that (8) has used the correct remote minority carrier boundary condition [4] in the $N_D \approx n_\infty$ term in (1), which has no negative f_ϕ as V_{gb} approaches V_{FB} . (8) can be solved exactly by numerical iteration, or explicitly by analytical approximations, as is widely used in ϕ_s -based bulk-MOS models.

CSM and ϕ_s Solution Near Flat-band

All contemporary bulk-MOS compact models employ the CSM [5] to overcome the mathematical difficulty in the second integration of the Poisson equation, or the (input) voltage equation (8), which basically equates the total gate (plus fixed oxide) charge to the induced charge in the channel/substrate (Q_{sc}) through charge neutrality:

$$C_{ox}(V_{gb} - V_{FB} - \phi_s) = Q_g + Q_{ox} = -Q_{sc} = \text{sgn}(\phi_s) C_{ox} \gamma \sqrt{f_\phi} \quad (9)$$

or, defining normalized (by C_{ox}) “charges,” $q_x \equiv Q_x/C_{ox}$, (9) is equivalent to (8):

$$V_{gb} - V_{FB} - \phi_s = q_g + q_{ox} = -q_{sc} = \text{sgn}(\phi_s) \gamma \sqrt{f_\phi}. \quad (9a)$$

The left-hand side (LHS) of (9) is described by ϕ_s , whereas the right-hand side (RHS) is non-integrable if doping (N_A) and either holes (p in accumulation) or electrons (n in inversion) are both present. The CSM attempts to separate the (mobile) inversion charge (Q_i) from the (fixed) depletion charge (Q_b): $Q_{sc} = Q_i + Q_b$, and by assuming a sheet of charge for Q_i and using depletion approximation for Q_b , terminal charges and currents can be integrated out across the channel of a MOSFET. However, in ϕ_s -based models, accurate solution of ϕ_s is essential, and none of the terms in (8) can be ignored near the flat-band voltage.

Iterative/Explicit ϕ_s Approach

The iterative approach (for bulk MOS) attempts to solve the full voltage equation (8) exactly through numerical methods; or by “iterating” a few times the approximated analytical equations from (8), or some mathematically “conditioned” form of (8). Either approach has been shown to give accurate and physical ϕ_s solutions. However, beyond the bulk-MOS equation (8), it is nontrivial to be extended to devices whose governing equations are given by (7) [or (3)–(5)] when the surface potential is coupled with the back-gate or mid-gap potential.

Essence of the Unified Regional Approach

Regional solutions to (8) can be easily obtained when f_ϕ is approximated regionally by

$$f_\phi = \begin{cases} e^{-\phi_s} & V_{gb} < V_{FB}, (p) \\ \phi_s & V_{FB} < V_{gb} < V_t, (N_A) \\ e^{\phi_s - 2\phi_F + \psi_{cb}} + \phi_B & V_{gb} > V_t, (n + N_A) \end{cases} \quad (10)$$

which has the following (piece-wise) solutions:

$$\phi_s \approx \begin{cases} \phi_{cc} = V_{gb} - V_{FB} + 2v_{th}\mathcal{L}\{w\} & V_{gb} < V_{FB} \\ \phi_{dd} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{FB}} \right)^2 & V_{FB} < V_{gb} < V_t \\ \phi_{ss} = \phi_{s0} + V_{cb} + \Delta & V_{gb} > V_t \end{cases} \quad (11)$$

The unified regional solutions

$$\phi_{s,eff} = \begin{cases} \phi_{acc} = V_{gbr} + 2v_{th}\mathcal{L}\{w\} & V_{gb} < V_{FB} \\ \phi_{sub} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gbf}} \right)^2 & V_{FB} < V_{gb} < V_t \\ \phi_{str} = \phi_{s0} + V_{cb} + \Delta_{eff} & V_{gb} > V_t \end{cases} \quad (12)$$

can be obtained [7] through two interpolation functions

$$V_{gbf} = \mathcal{G}_f \{x; \sigma_f\} \equiv 0.5 \left(x + \sqrt{x^2 + 4\sigma_f} \right) \quad (12a)$$

$$V_{gbr} = \mathcal{G}_r \{x; \sigma_a\} \equiv -0.5 \left(-x + \sqrt{x^2 + 4\sigma_a} \right). \quad (12b)$$

The key feature (or difference from iterative/explicit ϕ_s solution) is that the solution at flat-band is not solved exactly in each regional piece, but the combined one ($\phi_{sa} = \phi_{acc} + \phi_{sub}$) gives physical solution at flat-band, which can be easily tuned through two parameters (σ_a, σ_f) to meet the smoothness and charge neutrality at flat-band [7, 9]. Although the accuracy would not be as good as the iterative solution, the URM captures the essential physics asymptotically while avoiding the complicated solution near V_{FB} .

However, the single-piece unified $\phi_{s,eff}$ solution will not be used the same way as in ϕ_s -based models; rather, unified regional *charges* are the essence of the approach. This has been demonstrated in the bulk-charge (Q_b) modeling [7], which is based on the identity $V_{gb} - V_{FB} \equiv V_{gba} - V_{gbr}$ where V_{gba} is the “forward” interpolation function

$$V_{gba} = \mathcal{G}_f \{x; \sigma_a\} \equiv 0.5 \left(x + \sqrt{x^2 + 4\sigma_a} \right) \quad (12c)$$

($x = V_{gb} - V_{FB}$) having the same parameter (σ_a) as in V_{gbr} . This allows the LHS of (9) (gate charge) to be decomposed into the sum of accumulation and depletion charges:

$$\begin{aligned} Q_{sc} &= -C_{ox} (V_{gb} - V_{FB} - \phi_{sa}) \\ &= -C_{ox} \left[(V_{gba} + V_{gbr}) - (\phi_{acc} + \phi_{sub}) \right] = -C_{ox} \left[\underbrace{(V_{gbr} - \phi_{acc})}_{Q_{b,acc}} + \underbrace{(V_{gba} - \phi_{sub})}_{Q_{b,sub1}} \right] \\ &= Q_{b,acc} + Q_{b,sub} \end{aligned} \quad (13)$$

where

$$Q_{b,acc} \equiv -C_{ox}(V_{gbr} - \phi_{acc}) \quad (13a)$$

$$Q_{b,sub} \equiv -C_{ox}(V_{gba} - V_{gbf} + \gamma\sqrt{\phi_{sub}}) \quad (13b)$$

in which another (approximate) “identity” has been used:

$$V_{gbf} - \phi_{sub} = \gamma\sqrt{\phi_{sub}} \quad (13c)$$

due to the use of the same parameter (σ_f) in V_{gbf} and ϕ_{sub} . The $Q_{b,sub}$ defined above, which relates to the RHS of (8) (channel induced charge), is almost identical to the LHS of (8) $Q_{b,sub1} = -C_{ox}(V_{gba} - \phi_{sub})$ in the above derivation for bulk charge, as shown numerically by the difference ($< 10^{-11}$ % relative “error”), $\Delta Q_{b,sub} = |Q_{b,sub} - Q_{b,sub1}|$, in the inset of Fig. 4, which is always true for any device geometry and bias. With the complementary interpolation functions, the decomposed regional charges cross the flat-band smoothly (see Fig. 4), rather than “abruptly” as in ϕ_s -based CSM, which requires highly accurate solution close to the flat-band voltage.

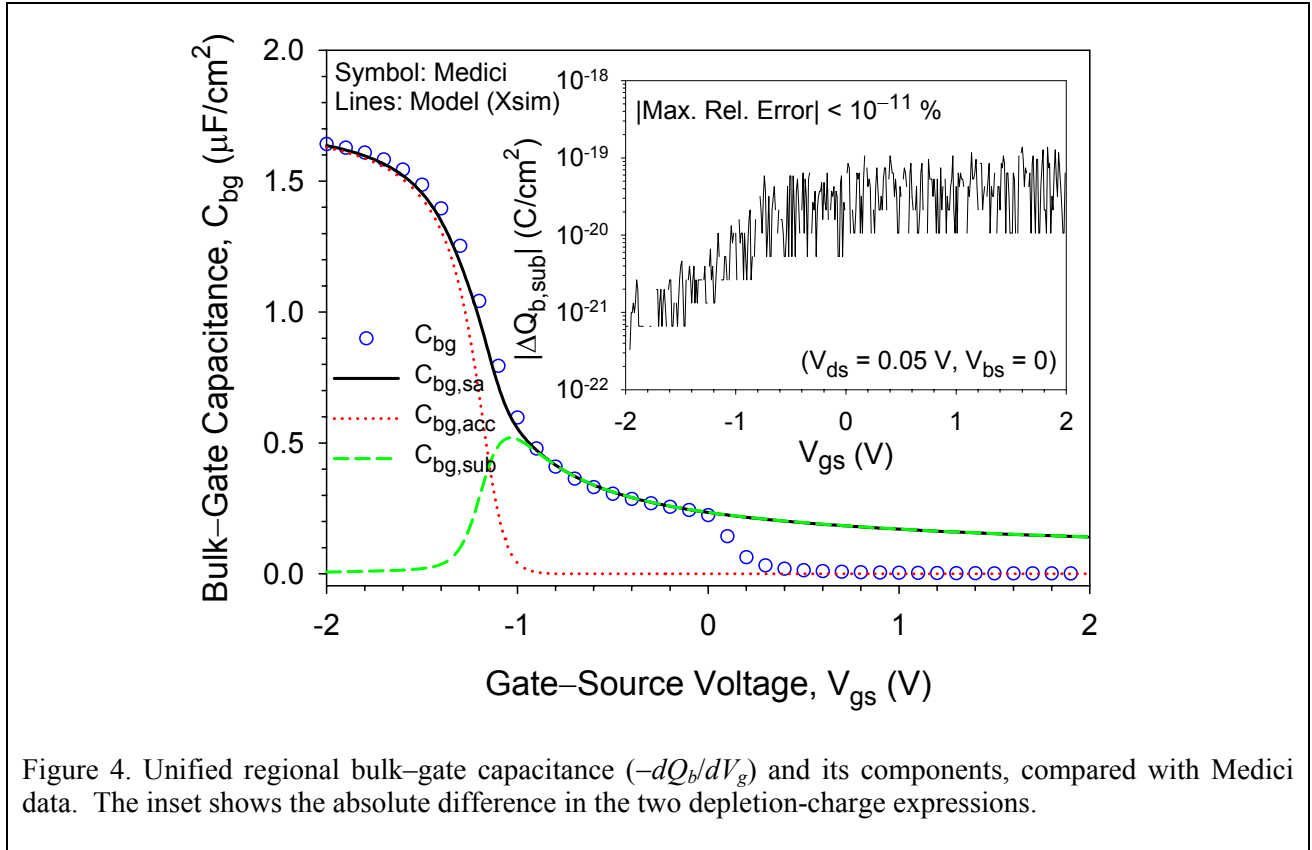


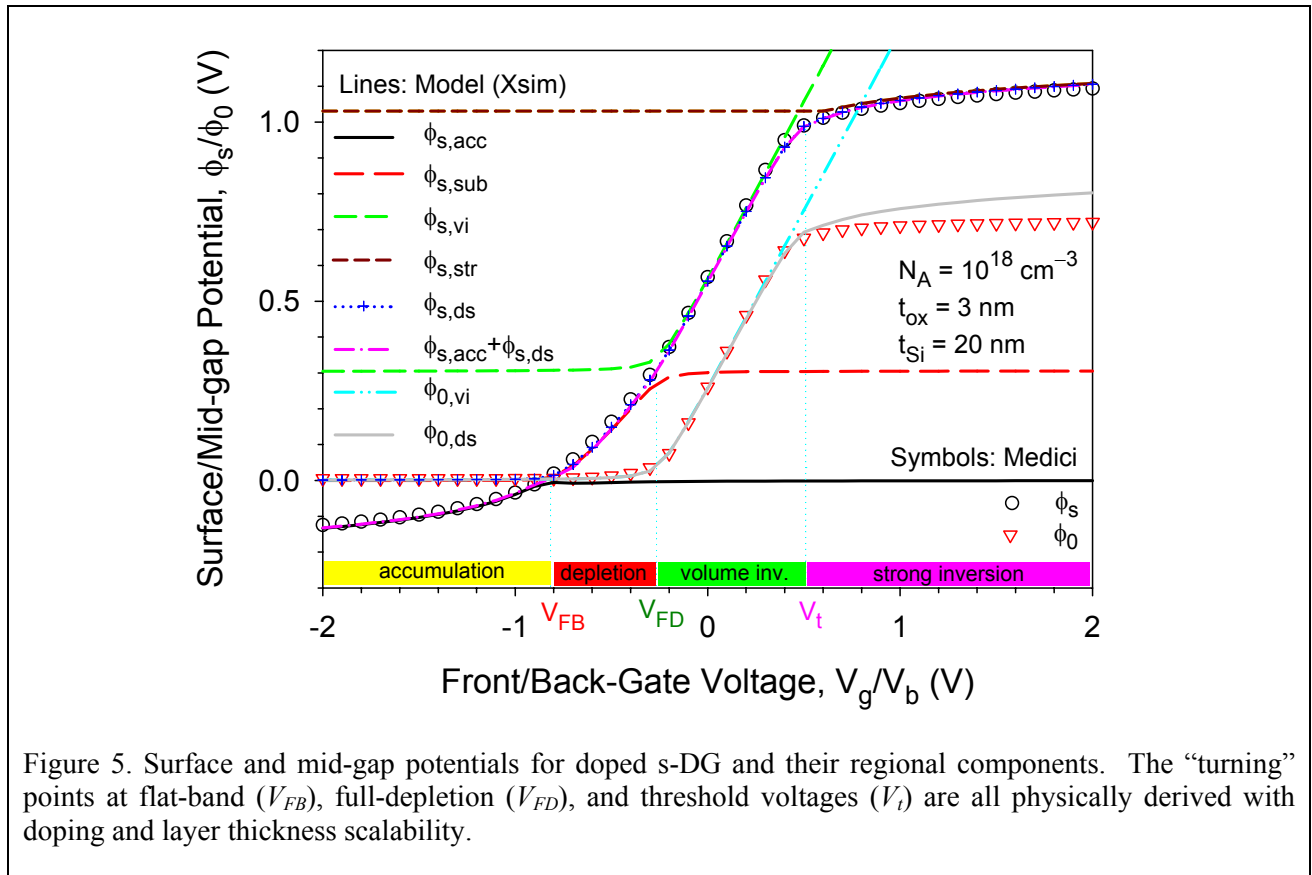
Figure 4. Unified regional bulk-gate capacitance ($-dQ_b/dV_g$) and its components, compared with Medici data. The inset shows the absolute difference in the two depletion-charge expressions.

Extending to SOI/DG MOSFETs

When extending the bulk model to SOI/DG MOSFETs, the advantages of the unified regional approach become apparent, since it will not be as “easy” (as for bulk), if not impossible, to solve the new voltage equations for the coupled front/back-gate or mid-gap potentials with the iterative/explicit SPM approach. Also, CSM fails when “volume inversion” occurs in UTB/FD-SOI/DG devices. However, with the URM approach, solutions to (7) are possible, as will be shown for the results in the next section.

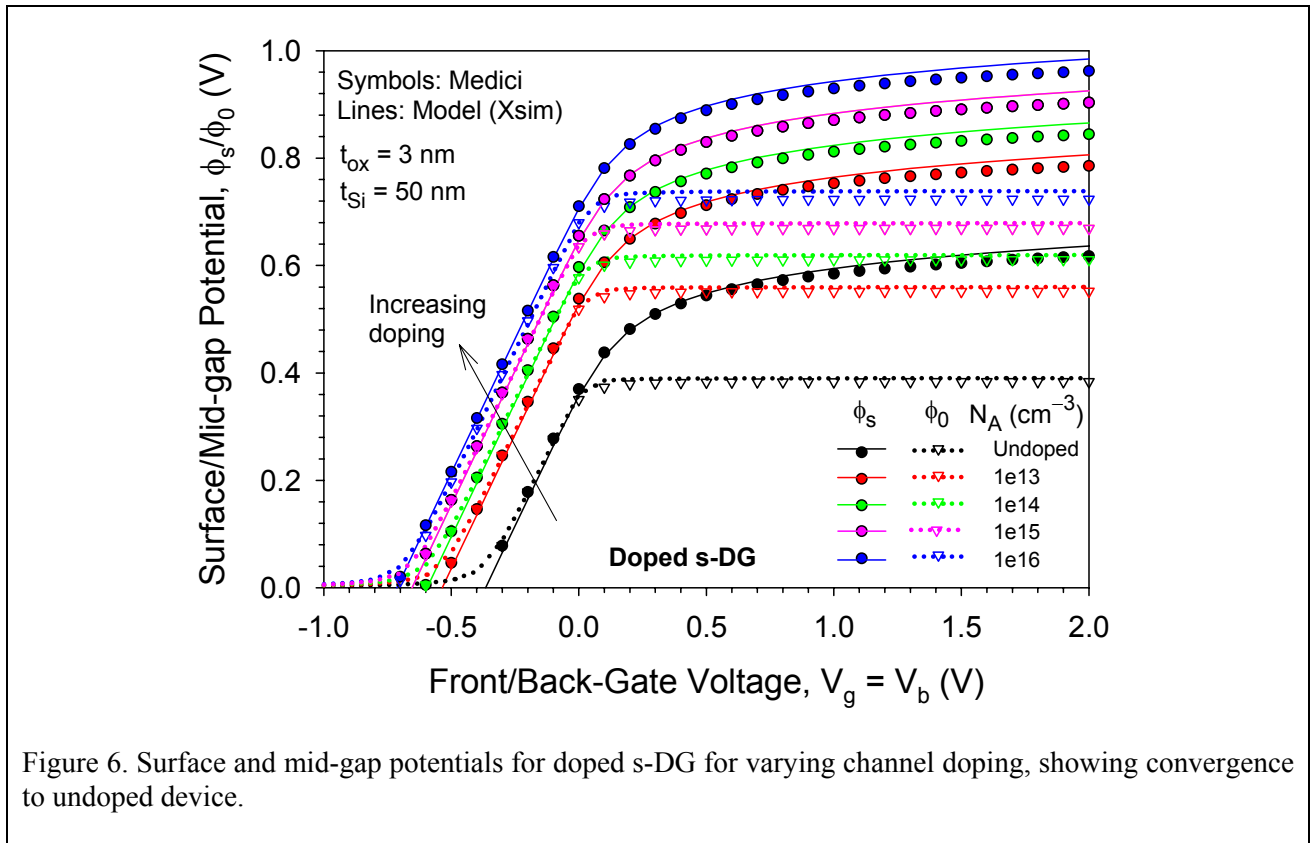
RESULTS OF VARIOUS STRUCTURES

In this section, we present our model results for various device structures compared with the same (ideal) numerical device from Medici, with an emphasis on the smooth/seamless transitions across device types and operations. Detailed formulations have been developed in [8] for doped s-DG based on URM approach, in [10] for undoped s-DG/a-DG/SOI based on Newton–Raphson (N–R) iterative method, and in [11] for undoped s-DG/a-DG/SOI based on explicit regional models. The most challenging task is to model the doped a-DG MOSFETs, which is our ongoing effort.



Doped s-DG/UTB/SOI MOSFETs

For s-DG (including bulk-UTB and FD-SOI with large t_{oxb}) MOSFETs in which $\phi'_0 = 0$ can be assumed, (7) is the governing equation, which is similar to the bulk-MOS voltage equation (8), if a relationship between ϕ_s and ϕ_0 can be found [8]. Figure 5 shows the regional solutions (in accumulation, depletion, weak/volume inversion, and strong inversion) of the surface and mid-gap potentials for a doped s-DG, as well as the unified solutions. Doping dependence in s-DG/UTB MOSFETs (above flat-band) is shown in Fig. 6 for the URM validated with Medici data, which demonstrates the importance of including doping (even unintentional) in DG structures, since the error (in mV range) in ϕ_s due to Fermi-level shift can be non-negligible if the model does not include the N_A term [8]. Channel thickness scaling is shown in Fig. 7 for the URM, in which total gate charge variation due to volume inversion is physically modeled. The model also converges to bulk as channel thickness increases.



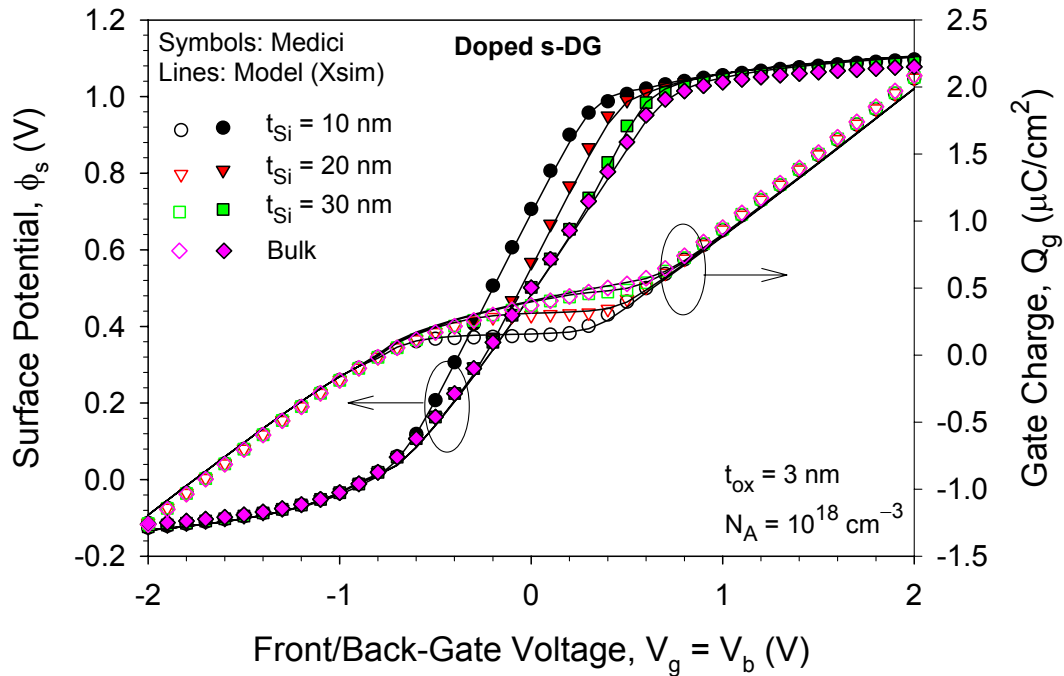


Figure 7. Surface potential and gate charge for doped s-DG/UTB at varying channel thickness, showing convergence to bulk device.

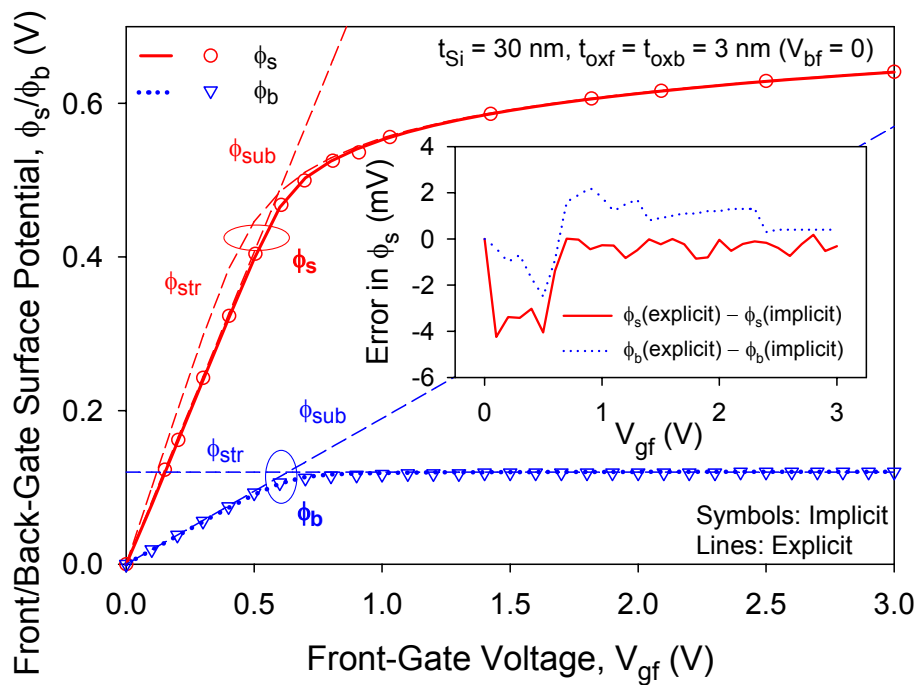
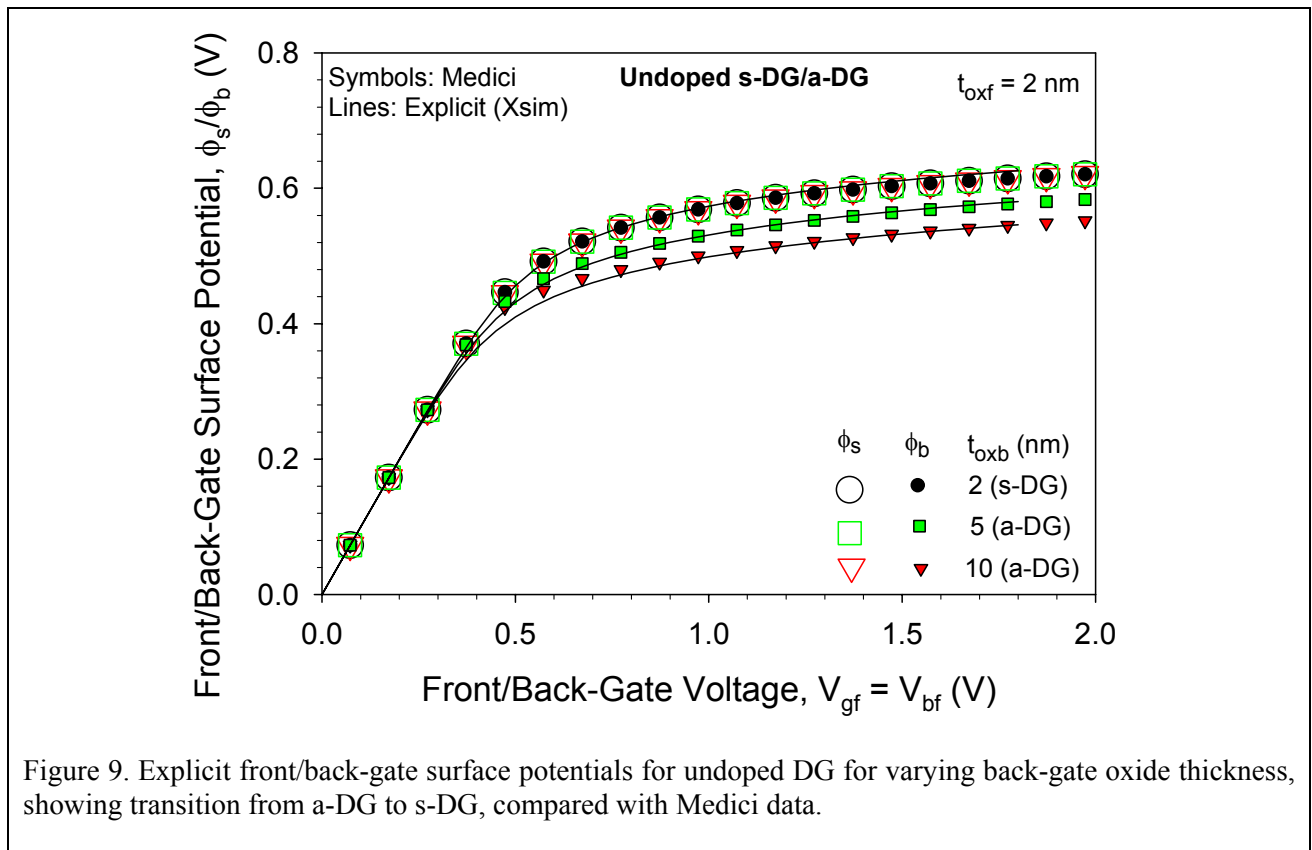


Figure 8. Explicit front/back-gate surface potentials for undoped a-DG and their regional components, compared with the implicit solutions. The inset shows the absolute errors of the explicit solutions.

Undoped s-DG/a-DG/SOI MOSFETs

For undoped DG/SOI MOSFETs, since the Poisson equation can be integrated twice [12], a generic solution with Newton–Raphson (N–R) iteration (with a very good initial guess) has been developed [10]. A URM approach has also been applied to undoped generic s-DG/a-DG/SOI devices [11]. Figure 8 shows the results of explicit regional front/back-gate surface-potential solutions for undoped a-DG, with the absolute errors shown in the inset. Transition from a-DG to s-DG is shown in Fig. 9 with the URM when both gates are tied together (so, asymmetry arises from varying back-gate oxide thickness). In Fig. 10 and Fig. 11, a-DG behaviors are well predicted by both the implicit and explicit solutions for t_{Si} and t_{oxb} variations, respectively, and verified in comparison with Medici data. Figure 12 shows the explicit surface potentials for two values of V_c , with < 6 mV error with respect to Medici, which are readily applicable in terminal-current evaluations at the source ($V_c = V_s$) and drain ($V_c = V_d$) sides.



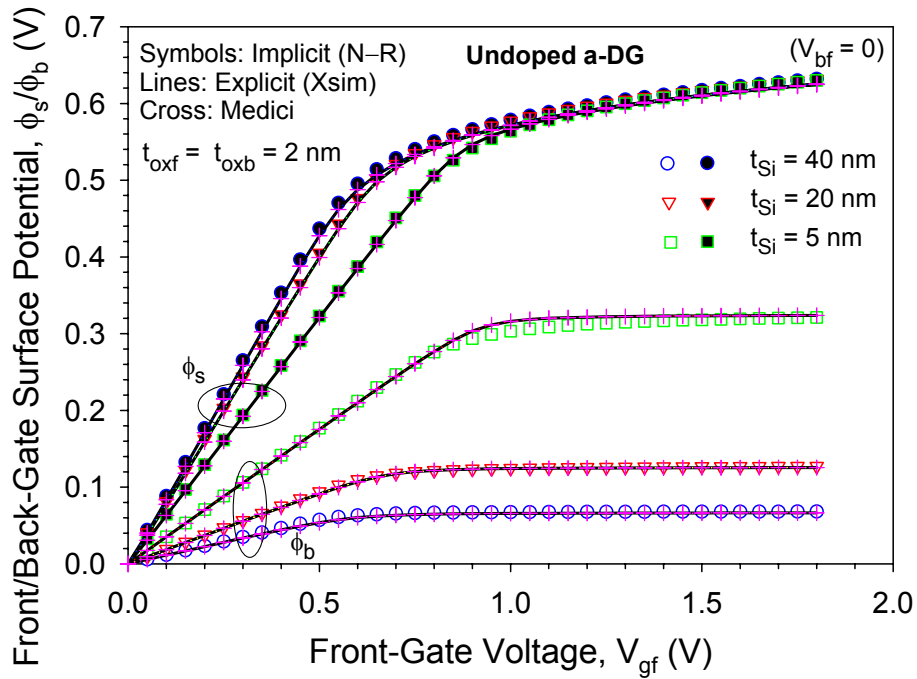


Figure 10. Front/back-gate surface potentials for undoped a-DG from implicit and explicit (regional) solutions for varying channel thickness, compared with Medici data.

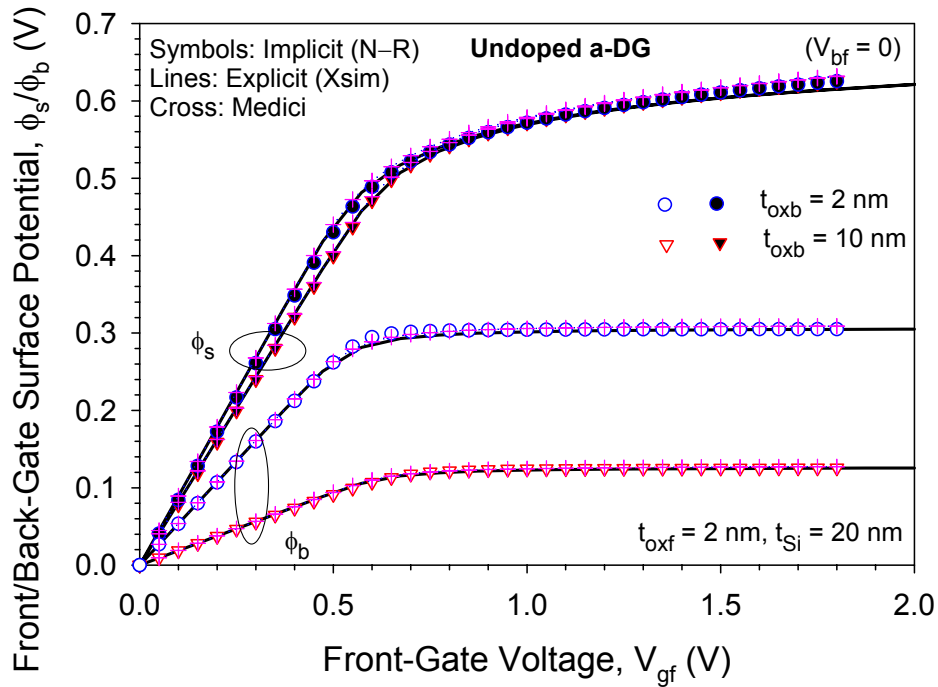
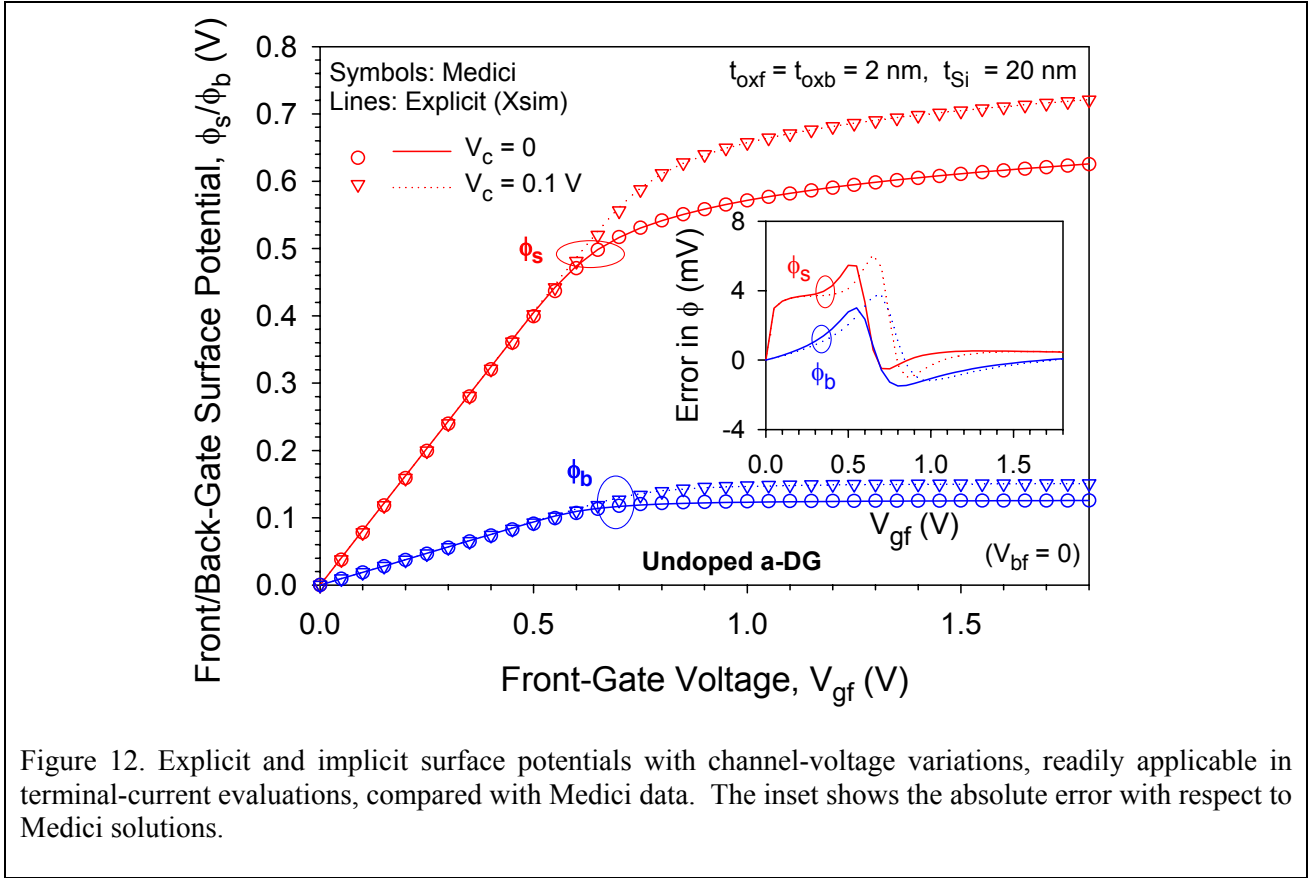


Figure 11. Front/back-gate surface potentials for undoped a-DG from implicit and explicit (regional) solutions for varying back-gate oxide thickness, compared with Medici data.



Doped a-DG/SOI MOSFETs

Doped a-DG (including FD-UTB SOI) MOSFETs represent the most challenging to model due to non-integrable (5) and highly sensitive coupling between the front- and back-gate surface potentials. With the URM approach, accumulation, depletion, and weak/volume inversion regions can be solved since the regional voltage equations are integrable. However, when the front gate is in strong inversion while sweeping the front-gate voltage at fixed back-gate bias, accurate ϕ_s solution is essential for solving ϕ_b , which is non-integrable. This remains the final challenge in our URM solutions for the generic MOSFET. However, once overcome, the approach and solutions would be generic and applicable for s-DG as well as undoped structures discussed previously. Our preliminary results for doped a-DG are shown in Figs. 13–16, in which back-gate oxide thickness dependence (from a-DG to FD-SOI) is shown in Fig. 13, channel-thickness dependence (from UTB to ‘bulk’) in Fig. 14, channel-doping dependence (from high doping to undoped) in Fig. 15, and back-gate bias dependence in Fig. 16, all physically scalable.

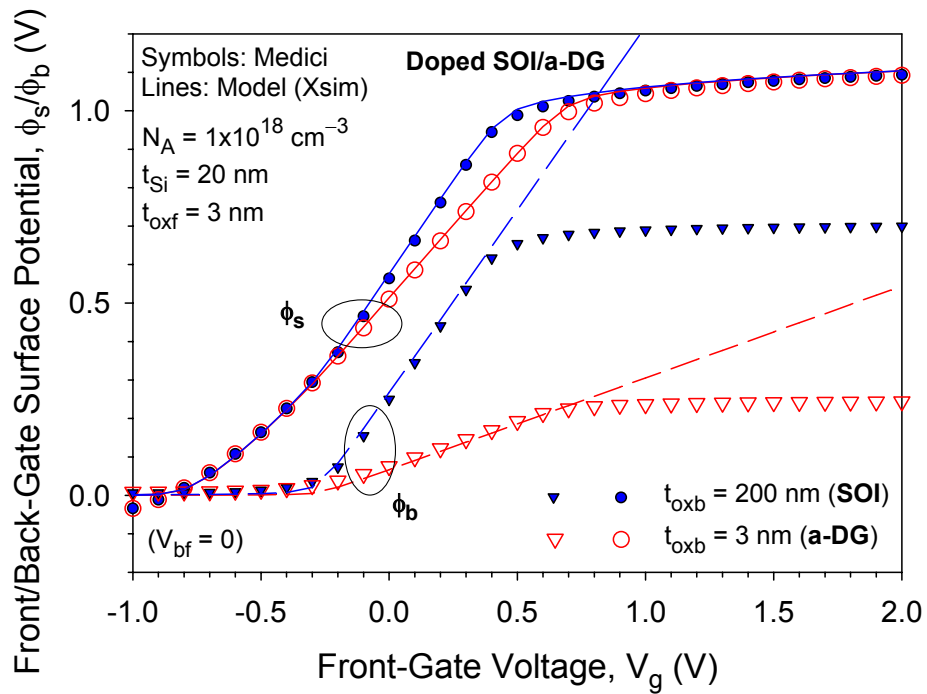


Figure 13. Explicit front/back-gate surface potentials for doped a-DG/SOI, showing physical scaling with back-gate oxide thickness, compared with Medici data.

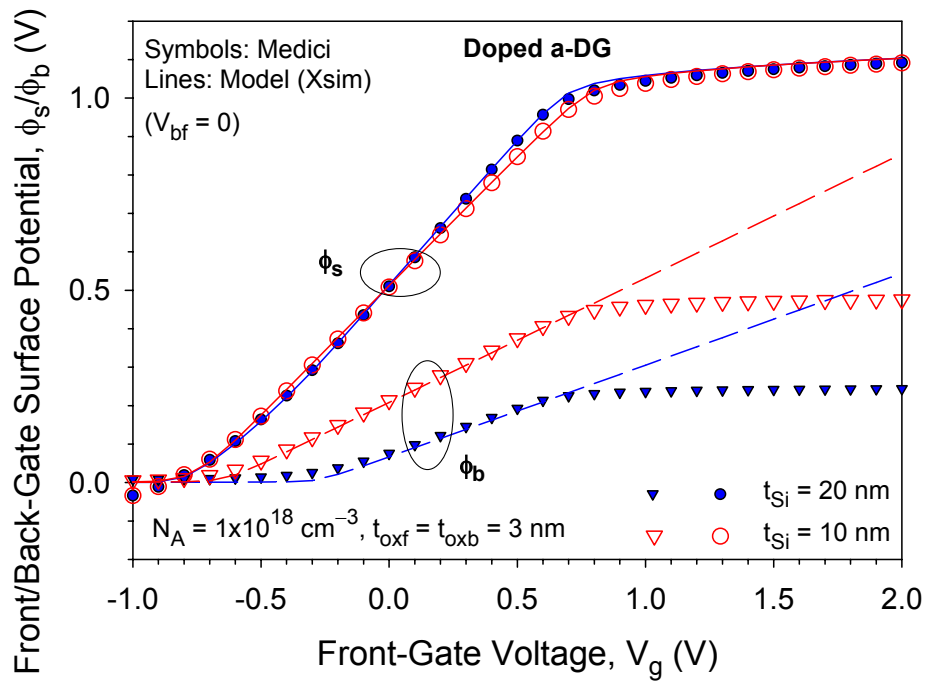


Figure 14. Explicit front/back-gate surface potentials for doped a-DG, showing physical scaling with channel thickness, compared with Medici data.

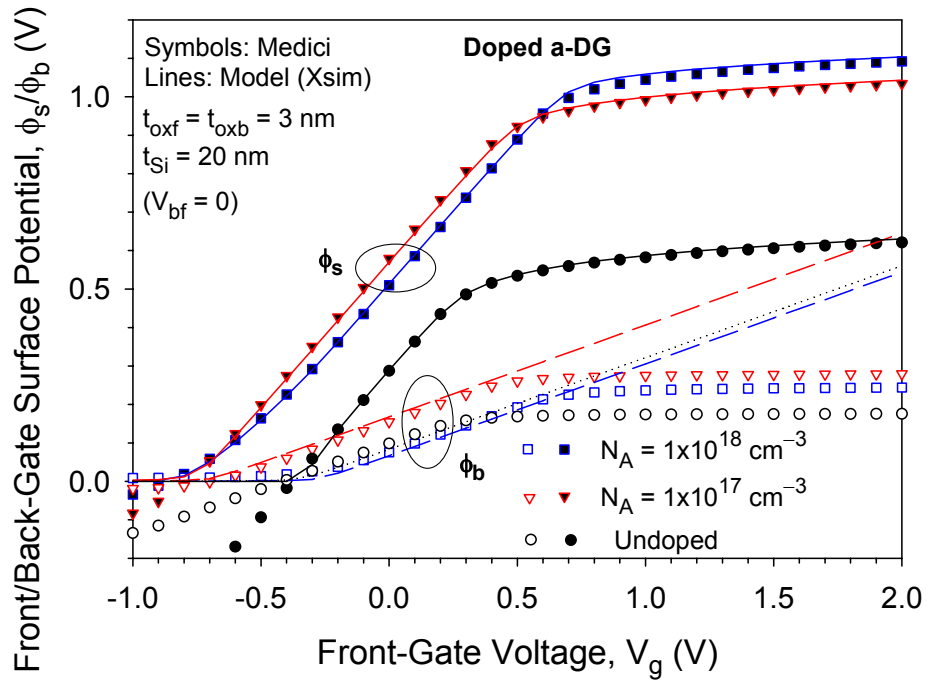


Figure 15. Explicit front/back-gate surface potentials for doped a-DG, showing physical scaling with channel doping (including undoped case), compared with Medici data.

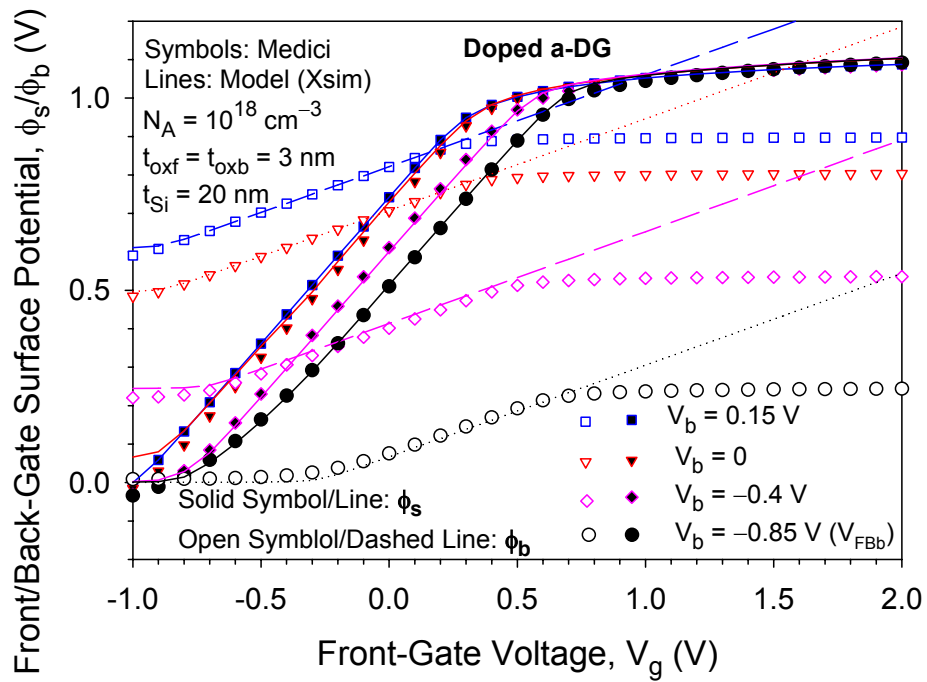


Figure 16. Explicit front/back-gate surface potentials for doped a-DG, showing physical scaling with back-gate bias, compared with Medici data.

SUMMARY AND CONCLUSIONS

Physical scalability and seamless transition over bias ranges (which is essential) and over geometry (which is critical) are fundamental requirements of a core model for circuit simulation. Model extension to various types of devices, such as existing bulk and SOI as well as emerging double-gate MOSFETs, may be only considered as a nice feature to have. However, seamless transition across device types and operations is a measure of the physics built in since transitions in real devices should really be seamless. The best of Einstein's theory is not only a brand *new* theory, but one that includes *old* (Newton's) theory as a special case. What have been proposed and demonstrated in this paper represents our efforts in building such a core model infrastructure in bridging today's modeling requirements with future generation modeling demands for non-classical devices as the building blocks to design integrated circuits. Although such a "dream" model is very challenging, it pays to have a forward-looking model as well as a dynamic approach. Finally, we quote Albert Einstein: "*Politics is for the present, but an equation is something for eternity.*"

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