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NEW COMPLEMENTARY BiCMOS DIGITAL GATES FOR LOW-VOLTAGE ENVIRONMENTS

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Abstract : A new generation of complementary BiCMOS digital gates for low-voltage environment will be presented. These include inverters and an AND gate. These circuits are particularly suitable for the scaled sub-half micrometer, 1.2 V BiCMOS generation and are designed to give full voltage swings at relatively high speeds. The number of devices used in the new circuit configuration is, by far, fewer than that in the recently reported circuits. The superiority of the new circuits has been confirmed by comparing their performance in terms of speed, voltage swing, power dissipation, noise margin and chip area, with the CMOS and that of the recently reported circuits. An analytical transient model for the basic circuit configuration is presented, and HSPICE simulations have been used to characterize the circuits. The experimental results obtained from the fabricated chip have also verified the functionality of the proposed circuit.

1. INTRODUCTION

Scaling of BiCMOS is inevitable for future VLSI applications where high packing density and low power dissipation are required [1,2]. However, the reduction of the power supply, demanded by reliability concerns and power consumption limitations, leads to a tremendous increase in the propagation delay [3,4] and a decrease in the output voltage swing [5]. To overcome these problems, an innovative approach is needed to design high speed, full-swing BiCMOS circuits for future low-voltage VLSI applications.

A few BiCMOS circuits for a low-voltage/low-power environment have been suggested [6, 8]. However, their performance features start to degrade for supply voltages less than 2 V. A 1.5 V full-swing BiCMOS circuit [9] has also been reported, but it uses too many devices, consumes a relatively large power, and has a large input capacitance.

This paper presents new full-swing BiCMOS circuits, particularly suited for the ~ 1.2 V supply operation. Section 2 describes the circuit operation and the main concepts involved. The experimental results are also shown in the same section. In Section 3, a detailed transient model is derived for the pull-up section of the circuit. Evaluation of the circuit performance and its comparison with the CMOS AND gate as derived from the new basic circuit configuration.

2. CIRCUIT DESCRIPTION, OPERATION AND EXPERIMENTAL RESULTS

The new circuit, shown in Fig. 1, is an improved version of Ref. [10]. The output stage utilizes complementary bipolar transistor Q_1 and Q_2 driven by a CMOS input stage. While the input to the circuit is applied to the common source, the state of the input CMOS stage, controlled by its gate voltage is determined by the feedback CMOS inverter, INV. For the pull up transition, a low (zero) output voltage would feedback a high voltage to the gate of the input stage thereby triggering N_1 ON. A low transition applied to the input causes N_1 to conduct, drawing its current from the conducting Q_1. The rising output voltage sends a transition, through the feedback inverter, to the gate voltage of N_1, eventually terminating the conduction of both N_1 and Q_1. Some of the charge, trapped in the saturated transistor Q_1 would find its way to the output and the output voltage. V_o increases further. Upon the beginning of a pull down phase, the remaining base charge is completely discharged through the substrate of N_1. This can be explained as follows: during the pull down cycle V_m changes from low to high causing the base-collector junction of the parasitic transistor, associated with N_1, to be forward biased thereby injecting the discharging current to the base of Q_1 as shown in Fig. 1. It should be noted that by establishing the proper gate voltage, the corresponding channels have been induced prior to the input transition and the two input drivers.