

IME



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MAJOR RESEARCH INTERESTS

Semiconductor device physics, materials and Integrated Circuits technology

- Advanced CMOS devices (SOI, strained Si/SiGe)
- High k dielectric
- Si based quantum structures

RECENT REPRESENTATIVE PUBLICATIONS

1. Dependence of Chemical Composition Ratio on Electrical Properties of HfO₂-Al₂O₃ Gate Dielectric

Moon Sig Joo, Byung Jin Cho, Chia Ching Yeo, Nan Wu, Hongyu Yu, Chunxiang Zhu, Ming Fu Li, Dim-Lee Kwong, and N.Balasubramanian, *Jap. Journal of Applied Physics* (in press).

2. *A Novel Approach for Integration of Dual Metal Gate Process Using Ultra Thin Aluminum Nitride Buffer Layer*

Chang Seo Park, Byung Jin Cho, Du An Yan, N.Balasubramanian, and Dim-Lee Kwong (to be presented in *VLSI Technology Symposium*, Japan, June 2003)

3. *Analysis of carrier generation lifetime in strained-Si / SiGe heterojunction MOSFETs from capacitance transient*

L.K.Bera, Shajan Mathew, N.Balasubramanian, G.Braithwaite, M.T.Currie, F.Singaporewala, J.Yap, R.Hammond, A.Lochtefeld, M.T.Bulsara, and E.A.Fitzgerald

(Presented in *International SiGe Technology and Device Meeting*, Jan 2003, Japan).

4. *Analysis of trace levels of Ge transferred to Si wafer surfaces during SiGe wafer processing*

L.K.Bera, Ajay Agarwal and N.Balasubramanian, *Electrochemical and Solid State Letters* **6**, G52, 2003.

5. *Effect of wafer backside clean process on the ULSI (ultra large scale integration) lithography*

N.Balasubramanian, M.M.Roy, Pauline and P.D.Foo, *Electrochemical Society Proceedings*, **Vol. 2002-2**, pp. 803-810, 2002.

6. *A partial SOI technology for single chip RF power amplifier*

Jun Cai, C.Ren, Y.C.Liang, N.Balasubramanian and J.K.O.Sin, *International Electron Device Meeting Digest*, pp. 891-894, 2001.

7. *Active corner engineering in the process integration for shallow trench isolation*

N.Balasubramanian, E.A.Johnson, I.V.Peidous, Shiu Ming-Jr and R.Sundaresan, *Journal of Vacuum Science & Technology B*, **Vol. 18**, 700 (2000).



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MAJOR RESEARCH INTERESTS

The scope of scientific/engineering activity is plasma etching (development and production) of all basic materials (mono and poly-silicon, silicon dioxide, silicon nitride, SOG, aluminum, Ti-W, tantalum, TaN, HfO₂, photoresist, low-k dielectrics, etc.) for VLSI silicon technology and in particular for copper dual damascene technology. This includes also studies of effect of plasma etch processes on the properties of dielectrics, metals and interfaces and on the yield and reliability of devices.

Teaching activity includes delivering lectures and on-site training in plasma etching equipment and processes for students and specialists and co-supervision of student master degree projects.

RECENT REPRESENTATIVE PUBLICATIONS

1. Vladimir Bliznetsov et al, "Plasma removal of post-RIE residues for dual damascene processing", *Proceedings of SPIE*, v. **4227**, pp.197- 204, 2000.
2. My The Doan, Vladimir Bliznetsov et al, "Precision resistor in a baseline 0.18 μm copper Interconnect". - *Proceedings of the 1st International Conference on Semiconductor Technology, ISTC 2001*, China, 27 - 30, 2001, v.2 pp.88 – 93.
3. Vladimir Bliznetsov et al, "Challenges in Etching of OSG Low- K Materials for Dual-Damascene Metallization", *Proceedings of Materials Research Society Symposium*, MRS 2002, v.**716**, p.331-336.
4. Vladimir Bliznetsov et al, "Reactive Ion Etching of Vias in Low-K OSG Films for Dual Damascene Technology", in *Book of abstracts of International Semiconductor Technology Conference ICTS 2002*.
5. Vladimir Bliznetsov et al, "Optimization of photoresist stripping for OSG low-k / copper damascene technology", *Proceedings of 2002 VMIC Conference*, p.483-486.
6. Yap Kuan Pei, Vladimir Bliznetsov et al, "Polymers Removal of Deep Trench Etch Process for Cu/Low-k RF Inductors" *Proceedings of 2002 VMIC Conference*, p.319-322.
7. Ahila Krishnamurthy, Vladimir Bliznetsov et al, "Effect of etching process deviations and type of photoresist stripping recipe on contact yield of copper dual damascene metallization", *Journal of Electrochemical Soc.*v.**149** (12) pp.G656-G660 (2002).
8. M.-M. Roy, Vladimir Bliznetsov et al, "A Dual BARC method for Lithography and Etch for Dual Damascene with Low K", to be published in *Jpn. J. Appl. Phys.* **Vol.42**, Part 1. No.5A, May 2003.



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MAJOR RESEARCH INTERESTS

In ultra large scale integration (ULSI) technology, there has been considerable interest in replacing conventional dielectrics SiO_2 with low-k ($k < 3.0$)/ultra low-k ($k < 2.4$) dielectrics to minimize the propagation delays. However, integration of low-k/Ultra low-k and its reliability is one of the grand challenges of the International Technology Roadmap Semiconductors for interconnect technology up to 2007 and beyond. Extensive process evaluation on all the integration and reliability issues has been completed in IME with the state of art equipments and many good solutions have been developed. For fundamental research, my interests currently focus on the mechanism of 1) Cu adhesion to low-k/ultra low-k materials with different process treatment and 2) Cu diffusion through barrier layer under high thermal stress from low-k materials. Surface physical/chemical properties of low-k/ultra low-k materials will be investigated by various methods, such as FTIR, TEM, TOF-SIMS, XPS, Auger to understand the interaction between different processes, such as etch & clean, and low-k/ultra low-k materials. Computation simulation based on quantum chemistry/physics will also be carried out to study above mentioned interaction at atomic level.

We are also interested in developing bio-sensors, combining the know-how and experience in ULSI Semiconductor Process Technology.

RECENT REPRESENTATIVE PUBLICATIONS

1. X. T. Chen, D. Lu, Y. T. Tan, Y. W. Chen, P. D. Foo. "Adhesion Enhancement in 0.13 μm Cu/Silk Integration", 2003 *Spring Materials Research Society*.
2. X. T. Chen, Y. T. Tan, Y. W. Chen, C. Y. Li, Ramana Murthy.B, S. Balakumar, Kevin Chew, P. D. Foo, "Delamination of Ta/SiLKTM in 0.13 μm Process Integration", *VLSI/ULSI MULTILEVEL INTERCONNECTION CONFERENCE (VMIC)*, 2002.
3. Chen Xian Tong, Prakash, Chai M.K., "Optimization of Contact Process to Improve Yield for 128/256Mg Devices", *3rd Tech Internal Technical Seminar*, 2001.



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MAJOR RESEARCH INTERESTS

1. BioMEMS process technology
2. Electrochemical Biosensors design, microfabrication and characterisations
3. Solid-state electrolytes, bio-materials, polymer and membrane technology in sensor application
4. Design, integration, microfabrication and characterisation of BioMEMS devices, microTAS system, microfluidic devices, biosensors and chemical sensors for life science, pharmacy, chemical engineering and environment application

RECENT REPRESENTATIVE PUBLICATIONS

1. Chen Yu, Zou Quanbo, Uppili Sridhour and Foo Pangdow, *Room Temperature Wafer-to-Wafer Bonding by Polydimethylsiloxane*, (US. **6503847**, 7-Jan-2003 granted)
2. Quanbo Zou; Uppili Sridhour; Chen Yu; Emmanuel Selvanayagam Zachariah; Yan Tie, *Miniaturized Thermal Cycler* (US. **6432695** 13 Aug. 2002 granted).
3. Chen Yu and Janak Singh, *Capillary with Glass Internal Surface*, (filed in U.S. Office 2002)
4. Zou Quanbo, Chen Yu, Janak Singh, Lim Tit Meng, Yan Tie and Heng Chew Kiat, *Single Wafer Fabrication of Integrated Micro-Fluidic System*, (filed in U.S. office, 2002)
5. Isabel Rodriguez; Marie Lesaichere, Yan Tie, Lim Tit Meng , Quanbo Zou, Chen Yu, Janak Singh, Chong Ser Choong, Sridhar Uppili and Z Emmanuel Selvanayagam, *Practical Integration of Polymerase Chain Reaction Amplification and Electrophoretic Analysis in Microfluidic Devices for genetic analysis*, *Electrophoresis* **24**, (2003). 172-178.
6. Zou Quanbo, Miao YuBo, Chen Yu, Uppili Sridhar, Chong Ser Chong, Chai Tai Chong, Yan Tie, Christina Hui Leng Teh, Tit Meng Lim, Chew Kiat Heng , *Micro-Assembled Multi-Chamber Thermal Cycler for Low-Cost Reaction Chip Thermal Multiplexing*, *Sensors and Actuators A* **102** (2002) 114-121
7. Chen Yu; Yubo Miao; Victor Sample; Fatimah Bte Mustafa; Qingxin Zhang; Chewkiat Heng; Huijen Lye; Titmeng Lim, *Microfabrication of Si Mesh Structure Depth Filter*, *MicroTAS 2002*, November 3-7, 2002, Nara, Japan.
8. Hongmiao Ji, Victor Samper, Wenmiao Shu, Qasem Ramadan, Chen Yu, *Microfluidic bead-based Valve*, *Eurosensor XVI*, 15 - 18 September 2002, Prague, Czech Republic
9. Qasem Ramadan , Victor Samper , Zhu Liang , Daniel Poenar Puiu , Lim Tit Meng, Heng Chew Kiat , Christina The, Chen Yu, *Microfluidic DNA Sample Preparation System by dielectrophoresis and Electroporation*, *Eurosensor XVI*, 15 - 18 September 2002, Prague, Czech Republic
10. Zou Quanbo, Sridhar Uppili, Chen Yu, Singh Janak; Emmanuel Seluanayagam; Tie Yan, Titmeng Lim; Isabel Rodriguez; Marie Laure Lesaichere , *A Micromachined Integrated Thermal Cycler*, *IEDM 2001*, 2 - 5 Dec 2001, Washington, USA



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MAJOR RESEARCH INTERESTS

Main Research areas:

1. RF and Bio-MEMS integration
2. Semiconductor Process development for PECVD and etching modules.
3. CMOS integration

Recent projects:

- Si microphone
- RF Micro-relay
- Microfluidic devices for nanoparticle detection
- Interposer for nano wafer level package
- Gate etch for 100nm NMOS and high K dielectrics

Patents:

1. Wang Zhe, Zhang Qing Xin, Feng Hanhua " A high performance silicon condenser microphone with perforated single crystal silicon back plate" filed with the US Patent Office in Sep 2002.
2. Wang Zhe, Zhang Qing Xin, Foo Pang Dow, Feng Hanhua " Apparatus and process for bulk wet etch with leakage protection" filed with Singapore Patent Office in March 2002.
3. Shuming Xu, Pang Dow Foo, Hanhua Feng " RF LDMOS on partial SOI substrate" US Patent 6461902 B1 (Date of award: 08-Oct-02).
4. Shuming Xu, Hanhua Feng, Pang Dow Foo, Bai Xu, Uppili Sridhar " Integrated Circuit Inductor" US Patent 6495903B3 (Date of award: 17-Dec-02).
5. Victor Donald Samper, Uppili Sridhar, Olaf Knueppel (Tyco), Feng Han Hua, Hui Wing Cheong, Dirk Wagenaar (Tyco) " Method to Prevent Charging Effects in electrostatic MEMS device" US Patent 6483223 (Date of award: 19-Nov-02).

RECENT REPRESENTATIVE PUBLICATIONS

1. L. K. Bera, Ranganathan. N, Feng Hanhua, R. Gopal; (2002): Chemical Analysis of resist residues formed during Polysilicon Gate Etch Process, *3rd International Conference on Microelectronics and Interfaces (ICMI)*, p. 236-238, Santa Clara, USA. Feb 11-14, 2002.
2. Quanbo Zou, Uppili Sridhar, Janak Singh, Ranganathan Nagarajan, Qingxin Zhang, Wenjiang Zeng, Xuexuan Qu, Hanhua Feng (2001) : *Ambient stable thermal bimorph actuator, iMEMS workshop 2001*, Singapore.
3. Z Wang, R. M. Lin, K. W. Leow, MK. Lin, S Uppili, H Feng. (2001): Design and simulation of a novel micromachined vibratory gyroscope with enhanced sensitivity performance. SPIE's MICRO/MEMS 2001, 17-19 December 2001, Australia. *Proceedings of SPIE Vol. 4593*, p.4593-16.
4. M.M Chiu, Man Wong, Yitshak Zohar, M. S. Tse, H. Feng and P. K. Chan, (1997) : Fabrication and Characterization of Polysilicon Temperature Microsensor. *International MEMS Workshop*, National University of Singapore, **15 & 16** November 1997, P.18-21.
5. Lavery, SJ., Feng, H., and Maguire, P., (1997): Adhesion of copper Electroplated to thin film tin oxide for electrodes in flat panel displays, *Journal of Electrochemistry Society* **144(6)**, 2165-2170.
6. Feng, H., Lavery, SJ., Maguire, P., Molloy, J., and Meenan B. J. (1996): Electrochemically Reduced Polycrystalline Tin Oxide Thin Films: Surface Analysis and Electroplated Copper Adhesion, *Journal of Electrochemistry Society* **143(6)**, 2048-2052.

7. Z. Xu, H. Ding, X. Zou, S. Zhang, H. Feng, Y. Dai, and X. Wan (1996): Back-propagation Neural Networks and its Application of PECVD SiN, *Integrated Optoelectronics*, Ray T. Chen, Won-Tien Tsang, Bingkun Zhou, Editors, Proceedings SPIE **2981** Supplement, 21-25.
8. Maguire, P., Feng, H., Molloy, J., Lavery, SJ., and McLaughlin, J. (1995): Patterning & Conductivity Enhancement of Transparent Electrodes for Flat Panel Display. *IEE Colloquium on Materials for Displays*, at Savoy Place, UK, 3 October 1995, P.11/1-11/6.
9. Feng, H. and Li, X. (1996):The Effects of Materials Coefficients on the Dispersion Characteristics of the Ferroelectric Domain Layer Wave. *Journal of Huazhong University of Science and Technology* **24**(Supplement 2), 48-51.
10. Feng, H. and Li, X. (1993):Shear-horizontal Surface Waves in a Layered Structure of Piezoelectric Ceramics. *IEEE Transaction on Ultrasonic Ferroelectric and Frequency Control* **40**, 167-170.
11. Feng, H. and Li, X. (1993):The Study on Electroacoustic Waves in Piezoelectric Layered Structure. *Piezoelectrics & Acoustooptics* **15**, 9-13.
12. Feng, H. and Li, X. (1992):The General Existence Conditions for the Ferroelectric Domain Layer Wave. *Ferroelectrics* **129**, 31-41.



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MAJOR RESEARCH INTERESTS

1. RF/MW components and devices design and modelling. RF/MW circuits design.
2. Fabrication of RF/MW components, devices, circuits and systems on semiconductor wafers.
3. Design and fabrication of RF/MW passives, circuits and systems in packaging level.

RECENT REPRESENTATIVE PUBLICATIONS

1. Guo Lihui, Yu Mingbin, Chen Zhen, He Han and Zhang Yi, "High Q Multi Layer Spiral Inductor on Silicon Chip for 5 ~ 6 GHz". *IEEE Electron Device Letters*, **Vol. 23, No. 8**, 2002, pp.470-472.
2. Chen Zhen, Guo Lihui, Yu Mingbin and Zhang Yi, "Study of MIMIM On-Chip Capacitor Using Cu/SiO₂ Interconnect Technology", *IEEE Trans on Microwave and Wireless Components Letters*, **Vol. 12, No. 7**, 2002, pp.246-248.
3. Chen Zhen and Guo Lihui, "Application of Genetic Algorithm in Modeling RF On-Chip Inductors", *IEEE Trans on Microwave Theory and Techniques*, **vol.51, No.2**, 2003, pp.342-346.
4. Guo Lihui, Yu Mingbin and Foo Pang Dow, "RF inductors and capacitors integrated on silicon chip by CMOS compatible Cu interconnect technology", *Microelectronics Reliability* **43** (2003) 367-370.
5. Sun Tietun, Miao Jianmin and Guo Lihui, "Development of micromachined RF silicon inductors" published on *The international MEMS workshop 2001*, 4-6 July 2001, Singapore, P.311-315.
6. Chen Zhen, Yu Mingbin and Guo Lihui, "Design and Fabrication of RF MEMS Switches on Silicon Substrates with Advanced IC Interconnect Technology", *The Sixth International Conference on Solid-State and Integrated-Circuit Technology*, October 22-25, 2001, Shanghai, China.
7. Longqing Chen, Jianmin Miao, Lihui Guo and Rongming Lin, "Control of stress in highly doped polysilicon multi-layer diaphragm structure", *Surface and Coating Technology* **141** (2001) P.96-102.



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MAJOR RESEARCH INTERESTS

Optical component packaging design
 Optical component reliability modeling and analysis
 Optical communication test-bed development
 Optical and electrical characterization for failure mode analysis
 RF device parameter extraction and reliability modeling
 Hot-Carrier and TDDDB related reliability and failure analysis.

RECENT REPRESENTATIVE PUBLICATIONS

1. N. Hwang, S.S.B. Or, and L. Forbes, "Tunneling and Thermal Emission of Electrons from a Distribution of Deep Traps in SiO₂," *IEEE Trans. on Electron Devices*, **Vol. 40**, No. 6, pp. 1100-1103, 1993.
2. N. Hwang and L. Forbes, "Hot-Carrier Induced Series Resistance Enhancement Model (HISREM) of nMOSFET's for Circuit Simulations and Reliability Projections," *Microelectron. Reliab.*, **Vol. 35**, No. 2, pp. 225-239, 1995.
3. N. Hwang, S.-G. Kang, H.-T. Lee, M.-K. Song, D.-G. Kim, and H.-M. Park, "Reliability Purge Test of SAGCM InGaAs/InP APD's," *IRPS*, 1995, pp. 187-190.
4. N. Hwang, S.-G. Kang, H.-T. Lee, M.-K. Song, and K.-E. Pyun, "Degradation Models and Lifetime Projections of InGaAs/InP MQW-DFB Laser Diodes for High-Speed Optical Communication Systems," *IRPS*, 1996, p. 195.
5. N. Hwang, S.-G. Kang, H.-T. Lee, S.-S. Park, M.-K. Song, and K.-E. Pyun, "An Empirical Lifetime Projection Method for Laser Diode Degradation," *IRPS*, 1997, pp. 272-275.
6. N. Hwang, H.-S. Cho, H.-T. Lee, M.-K. Song, H.-M. Kim, and K.-E. Pyun, "Lifetime projection and degradation mechanism of 1.3- μ m InGaAsP/InP uncooled laser diodes," *OFC'97 Technical Digest*, Dallas, TX., **WL55**, pp. 222-223, Feb. 16-21, 1997.
7. N. Hwang, J.-T. Moon, M.-K. Song, and K.-E. Pyun, "A Novel Reliability Projection Model of Semiconductor Laser Diodes by Correlating Thermal Characteristics with Long-Term Degradation," *IRPS*, 1998.
8. N. Hwang, S.H. Lee, G.C. Joo, M.K. Song, and K.E. Pyun, "Relationship Between Initial Thermal Characteristics and Lifetime Projection of Semiconductor Laser Diodes," *Electronic Components & Technology Conference, 1998*. 48th IEEE , pp. 1422-1423, 1998.
9. D.K. Oh, M.G. Kim, H.S. Kim, N. Hwang, H.-T. Lee, K.-E. Pyun, and C.D. Park, "Fabrication and Characterization of Complex-Coupled MQW-DFB Laser with an InGaAs Absorptive Grating," *Journal of Korean Physical Society*, **vol. 34**, pp. S92-S95, Apr. 1999.
10. S.G. Kang, M.K. Song, S.S. Park, S.H. Lee, N. Hwang, H.T. Lee, K.R. Oh, G.C. Joo, and D.H. Lee, "Fabrication of Semiconductor Optical Switch Module Using Laser Welding Technique," *IEEE Trans. Advanced Packaging*, **vol. 23**, **no. 4**, pp. 672-680, Nov. 2000.
11. G.C. Joo, S.H. Lee, K.S. Park, S.S. Park, J.S. Choi, N. Hwang, and M.K. Song, "A Novel Bidirectional Optical Coupling Module for Subscribers," *IEEE Trans. Advanced Packaging*, **vol. 23**, **no. 4**, pp. 681-685, Nov. 2000.
12. N. Hwang, "Failure Analysis of 10~13 GHz Phase Shifter MMICs," *Journal of Korean Physical Society*, **vol. 39**, pp. S131-S133, Dec. 2001.
13. K.H. Oh, N. Hwang, J.S. Koh, "Optical Pulse Characteristics of a Gain Switched GaAs VCSEL Operating at 850 nm Wavelength," 7th Optoelectronics and Communications Conference (OECC 2002) *Technical Digest*, Kanagawa, Japan, July 8-12, 2002



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MAJOR RESEARCH INTERESTS

- 1) Design & Development of RF & Photonic interconnects and modules.
- 2) System in Package (Silicon, Organic & Photonic modules) – Design & Development

RECENT REPRESENTATIVE PUBLICATIONS

- 1) M.K. Iyer et.al; Design optimization for 10Gbps ElectroAbsorption Modulator LD packaging to appear in *Proc of IEEE 53rd Electronic Components Technology Conference*, New Orleans USA 27-30, May 2003
- 2) M.K. Iyer et.al ; Design and electrical characterization of a novel Wafer Level package for RF MEMS applications, to appear in *Proc of IEEE 53rd Electronic Components Technology Conference*, New Orleans, USA 27-30 May 2003
- 3) M.K. Iyer et.al ; Addressing Packaging Challenges ; *IEEE Circuits & Devices* ; **Vol 18**, No 4, July 2002
- 4) M.K. Iyer et.al ; System –in Package : Electronics, Photonics & MEMS modules integration
Invited Paper – *IEEE/ IMAPS Proc of International Conference on Electronic Packaging*, Tokyo, Japan April 2002
- 5) M.K. Iyer et.al ; A novel wirebonded plastic chip package for RF and Microwave applications, Proc of IEEE - *52nd Electronic Components & Technology Conference (ECTC)*, San Diego, CA, USA May 2002.
- 6) M.K. Iyer et.al ; A new modeling concept for high frequency characterization of multilayer packages , *IEEE CPMT - Transactions on Advanced Packaging* , **Vol 21**, No 3, March 2001.



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MAJOR RESEARCH INTERESTS

Wafer Level Interconnects & packaging

Nano materials & Nano interconnects

Wafer to wafer bonding

Silicon Through wafer interconnects

Silicon Micro modules for System in Package (SiP) Integration

Cu/Ultra low-k integration and packaging (Wire bonding & Flip Chip)

RECENT REPRESENTATIVE PUBLICATIONS

1. Kripesh, V. et. al (2002) Reliability of wire bonding on low-k dielectric material in damascene copper integrated circuits, *Microelectronics Reliability*, **42**, 1535-1540.
2. Kripesh, V et. al (2002) Selective Electroless Plating of Copper on (100)-Oriented Single Crystal Silicon Surface Modified by UV-Induced Coupling of 4-Vinylpyridine with the H-Terminated Silicon, *J. Physical Chemistry B*, **106**, 12508-12516
3. Kripesh, V et. al (2002) Wire bonding Process Impact on Low-K dielectric Material in Dual Damascene Copper Integrated Circuits” Proceeding of 52nd ECTC Conference, US, 31st May 2002
4. Kripesh, V et. al (2002) "Fine Pitch Wire Bond Dual Damascene Copper Chip PBGA Assembly and its Reliability Performance ", Proceeding of ICEP 2002, Japan, 15th April 2002.
5. Kripesh, V et. al (2002) Fine Pitch Copper Wire Bond Process Development for Dual Damascene Cu metallized chips”, Proceeding of EPTC conference, Singapore December 2002.
6. Kripesh, V et. al (2002) "Process characterization for oxide removal and cleaning of Cu metallized chips for wire bonding Applications", Proceedings of Semicon 2002, Singapore, 7th May 2002.
7. Kripesh, V et. al (2002) “Thermal Aging Behavior of Pb-free Solders in CSP Packages” Proceeding of SEMICON 2002, 7 May 2002. **(BEST PAPER AWARD)**



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MAJOR RESEARCH INTERESTS

Back end of the line interconnects – integration and reliability

Process integration and electrical characterization

Yield analysis and improvement

Reliability of copper-low k and copper-ultra low k interconnects

Electromigration

Dielectric breakdown

Stress migration

Failure analysis to characterize reliability failures at surface / interface

Reliability improvement by process modifications

RECENT REPRESENTATIVE PUBLICATIONS

Two US patents

1. Metallization structures for microelectronic applications and process for forming the structures, United States Patent 6,368,966 dated April 9, 2002.
2. Copper alloy electroplating for microelectronic applications, United States Patent 6,319,387 dated November 20, 2001

Journal / conference publications

1. Effect of etching process deviations and photoresist stripping on contact yield of copper dual damascene metallization
Ahila Krishnamoorthy, Vladimir Bliznetsov, Hui Leng Tay, and Bo Yu
J. Electrochem. Society, **149** (12) p. (2002)
2. Self-assembled near-zero-thickness molecular layers as diffusion barriers for Cu metallization
Krishnamoorthy, K. Chanda, S.P. Murarka, G. Ramanath, and J.G. Ryan
Applied Physics Letters, **78** (17) 2001, pp. 2467-2469.
3. A tertiary current distribution model for the pulse plating of copper into high aspect ratio sub-0.25 μ m trenches
D. Varadarajan, C.Y. Lee, A. Krishnamoorthy, D.J. Duquette and W. N. Gill,
J. Electrochemical Society, **147** (9) 2000, pp. 3382-3392.
4. Demonstration of Cu-Coral dual damascene process integration
Dielectric breakdown and reliability in copper-Black Diamond damascene structures
Effect of surface treatment on electromigration in sub-micron Cu damascene lines
Study of leakage mechanisms of copper/Black Diamond damascene process
Effect of ramp rate on breakdown of Black Diamond in copper damascene structure
International Conference on Materials for Advanced Technologies (ICMAT) Symposium L, 29th June to 4th July, Singapore.

5. Assessment of reliability of Cu-Black Diamond interconnects using time dependent dielectric Breakdown Asymmetry of electromigraton lifetime of upper layer and lower layer Cu line in Cu dual damascene process }
Materials Research Society Spring Meeting, 21-25 April, San Francisco.
6. Yield investigation in the integration of Cu/Black Diamond dual damascene interconnect
International Semiconductor Technology Conference, Sept. 12-14, 2002, Japan.
7. Demonstration of dual damascene 0.18 μm Cu/Black Diamond integration, Resistance degradation profile in electromigration of dual damascene Cu interconnects }
 Yield study of Cu/Black Diamond dual damascene interconnects using burn-in
Advanced Metallization Conference, Oct. 1 – 3, 2002, San Diego, USA.
8. Impact of via and upper layer formation on electromigration failure mechanism of lower layers in dual damascene Cu interconnects }
 Critical issues in the integration of Copper-Black Diamond interconnects
 Yield analysis of Cross-bridge Kelvin via resistors
2002 VMIC – Nineteenth International VLSI Multilevel Interconnection Conference, Nov. 18 to 20, 2002, Singapore.



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MAJOR RESEARCH INTERESTS

- Electronic Materials Science and Technology
 - Alternative IC gate dielectrics, Interconnect Technology, III-V compound applications.
- Material and Advanced Process & Assembly Characterization and Analysis
 - Deep submicron process, electronic package & assembly process
- Surface & Interface Analytical Technology and Applications (XPS/AES/SIMS/XTEM)
- Operation & Technology Roadmapping

NOTABLE ACHIEVEMENTS

- have published > 60 publications in referred journals and conference proceedings.
- have visited > 15 developed countries for scientific research and industry development project presentation.
- Have trained > 25 students in their master's and doctorate's program.
- have consulted > 75 companies in and around Singapore for QA/FA and yield improvement.
- Have organised/conducted >10 forums/workshops on Science & Technology fields.
- Founded and supporting user group platforms for R&D collaboration and BiZ relevancy enhancement
 - Singapore Focussed ion beam Application Group (SFAG).
 - Singapore Surface & Interface Analysis Group (SSAIG).
 - Singapore Analytical & Test Service Providers Group (SATS-PG).

RECENT REPRESENTATIVE PUBLICATIONS

1. Changhong Chen, Weiguang Zhu, Ting Yu, Xiaofeng Chen, Xi yao, R. Gopal Krishnan (2003) Surface and Coatings Technology 167, 245-248.
2. Choy Siew Fong, Vanissa Lim Sei wei, R. Gopal Krishnan, Alastair Trigg, LK Bera, Shajan Matthew, N. Balasubramanian, Joo Moon Sig, Byung Jin Cho and Yeo Chia Ching. *Proceedings of International Conference on characterization and metrology for ULSI technology* (Mar 2003, USA) - accepted
3. Rajinish K. Sharma, Jiang Ning, Han Hua and R. Gopalakrishnan *MRS Fall Meeting (Dec 2002, USA)* - (accepted)
4. Priya Naidu, R. Gopal Krishnan, Leong Siew Yong, Khine Nyunt and Richard Thet Wyan *19th VLIC/ULSI Multilevel Interconnection Conference Proceedings*, Singapore (2002) 67-71
5. YF. Chong, R. Gopalakrishnan , C F Tsang, G. Sarkar, S. Lim and S. Tatti (2001) J. Electronic Materials 30, 275-282.



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MAJOR RESEARCH INTERESTS

His research interest is on Si based heterostructure materials/devices. These includes:

- Strained-Si, SiGe and partially strained compensated SiGeC alloy films.
- The growth and characterisation of Ultra-Thin Gate Oxide and its reliability studies on Si, SiGe, strained-Si and SiGeC using microwave plasma CVD, ECR PECVD and conventional thermal process.
- Device (n/p MOSFETs) fabrication and characterisation on strained-Si.
- Process and device physics on sub-100 nm MOS device
- Junction and schottky diodes analysis on $\text{Si}_{1-x}\text{Ge}_x$ and strained-Si.
- Process development for ultra thin (EOT $\sim 1.0\text{nm}$) high-K gate dielectrics
- Si/Ge/SiGe quantum dot synthesis by self assemble method and its characterisation
- Device (memory device) fabrication and characterisation
- Si/SiGe based optical device (photo detector, laser etc)
- Metal gate process for n/p MOS

RECENT REPRESENTATIVE PUBLICATIONS

1. L.K.Bera, Ajay Agarwal and N.Balasubramanian, "Analysis of trace Ge concentration on Si surface during SiGe wafer processing", *Electrochemical and Solid-state Letters*, April-2003
2. L.K.Bera, Shajan Mathew and N.Balasubramanian, G. Braithwaite, M.T. Currie, F. Singaporewala, J. Yap, R. Hammond, A. Lochtefeld, M. T. Bulsara, and E. A. Fitzgerald "Analysis of carrier generation lifetime in strained-Si / SiGe heterojunction MOSFETs from capacitance transient" ISTDM-2003, Japan (accepted for publication in *Appl. Surface Science*)
3. L.K.Bera, Shajan Mathew, N.Balasubramanian, C. Leitz, G. Braithwaite, J. Carlin, T. Langdo, T. Lochtefeld, M. Currie, R. Hammond, J. Fiorenza, H. Badawi, and M. Bulsara "Investigation on furnace grown gate oxide on strained-Si" accepted in *2nd International conference on materials for advanced technologies (ICMAT)* June-Jul 2003, Singapore.
4. Shajan Mathew, L K Bera, Du An Yan, N Balasubramanian, G. Braithwaite, T. Lochtefeld, M. Currie, R. Hammond, J. Carlin, T. Langdo, C. Leitz, H. Badawi, and M. Bulsara "Investigation of diode leakage in n+/p junctions formed on strained silicon grown on $\text{Si}_{0.7}\text{Ge}_{0.3}$ buffer layers" accepted in *2nd International conference on materials for advanced technologies (ICMAT)* June-Jul 2003, Singapore.
5. H.Y. Yu, H.F. Lim, J.H. Chen, M.F. Li, C.X. Zhu, D.-L. Kwong, C.H. Tung, K.L. Bera, and C.J. Leo, "Robust HfN Metal Gate Electrode for Advanced MOS Devices Application" Accepted in *VLSI symposium-2003*

Patents:

A Low temperature resist trimming process, Ranganathan Nagarajan, Shajan Mathew and Lakshmikant Bera



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MAJOR RESEARCH INTERESTS

1. Analysis of organic contamination on wafer surfaces: FITR, GC-MS and ToF-SIMS are used to detect the presence or organic contamination on various wafer surfaces. The mechanism of the build-up of the organic contamination and its effects are also investigated.
2. Thermal stability of polymer low k materials: Various thermal analysis techniques and thermal desorption-GC-MS are used to study the thermal stability and thermal degradation of polymer low k materials. The change in the chemical structures of the polymer low k materials with temperature and its effects on the dielectric constant are also the focus of our research.
3. Study of the structure and properties relationship of high-performance organic fibers: Raman spectroscopy and transmission electron microscopy (TEM) are used to study the relationship between the micro-structure of the high performance organic fibers and their mechanical properties.

RECENT REPRESENTATIVE PUBLICATIONS

1. A.Y. Du, C.H. Tung, D. Lu, D. Gui and Y.F. Chow, (2002) The organic low-k materials microstructure study, *9th International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 179-182.
2. D. Lu and Z.X. Xing, (2002) Study of the thermal stability of an organic polymer low-k material, *International Journal of Modern Physics B* **(16)** 4441-4444.
3. Y. Li, S.C. Ng, L.K. Tan and D. Lu, (1997) Structure, properties and responses to heat treatment of melt-spun Cu-Y alloys, *Journal of Alloys and Compounds* **(259)** 276-282.
4. D. Lu, R.J. Young and M.C. Andrews, (1997) Compressive properties of aramid fibres", *Polymer* **38(10)** 2379-2388.
5. X. Hu, Q. Lin, A.F. Yee and D. Lu, X. Hu, Q. Lin, A.F. Yee and D. Lu, (1997) Structure and morphology of the in situ composite of a liquid crystalline polymer and polycarbonate, *Journal of Microscopy*, **(185)** 109-116.
6. X. Hu, Q. Lin, A.F. Yee and D. Lu, (1996) Skin-core morphology of in situ composites based on polycarbonate and a liquid crystalline polymer, *Journal of Materials Science Letters*, **(15)** 277-81.
7. B.X. Yang, Y. Zhu, J. Ahn, H.S. Tan and D. Lu, (1995) Growth and morphological studies of (100) textured diamond thin films by microwave plasma-enhanced chemical vapour deposition, *Thin Solid Films* **(270)** 210-214.
8. Li Tang, Dong Lu and Gareth Thomas (1995) Transmission electron microscopy study of microstructure and [1120]/[001] polycrystalline epitaxy of CoNiCr/Cr bilayer films, *Journal of Applied Physics* **77(1)** 47-53.
9. R. J. Young, D. Lu, R.J. Day, W.F. Knoff and H.A. Davies, (1992) Relationship between structure and mechanical properties for aramid fibres, *Journal of Materials Science*, **(27)** 5431-5440.
10. R.J. Young, D. Lu and R.J. Day, (1991) Raman spectroscopy of Kevlar fibres during deformation, *Polymer International*, **(24)** 71-76.



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MAJOR RESEARCH INTERESTS

- (i) Semiconductor Device Modelling for circuit design applications with emphasis on RF models for active and passive devices.
- (ii) Test structure designs and semiconductor device design.
- (iii) Semiconductor Device Physics

RECENT REPRESENTATIVE PUBLICATIONS

1. S. C. Rustagi, Huailin Liao, Jing Lin Shi and Yong Zhong Xiong, "BSIM3 RF Models for MOS Transistors: A Novel Technique for Substrate Network Extraction", *IEEE International Conference on Microelectronics Test Structures (ICMTS)*, 17-20 March, 2003, pp. 118-123.
2. S.C. Rustagi and Tan Chun Geik, "Equivalent Circuit Models for stacked Spiral Inductors in Deep submicron CMOS Technology", to be presented at *IEEE, ISCAS-2003*.
3. Huailin Liao, S. C. Rustagi, Jing Lin Shi and Yong Zhong Xiong, "Characterization and Modeling of the Substrate Noise and Its Impact on the Phase Noise of VCO" To be presented at *IEEE-RFIC-2003*.
4. S.C. Rustagi and C.C.C. Leung, "Accumulation Mode MOS varactor SPICE model for RFIC Applications" *Electronics Letters*, **Vol. 36**, No. 20, pp. 1735-36, 28th Sept. 2000.



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MAJOR RESEARCH INTERESTS

MEMS (Micro Systems Technology, Microsensors and Micro Devices)

- ↳ Biomedical applications of MEMS (BioMEMS)
 - ↳ Lab-on-chip and microfluidic biomedical systems
 - ↳ Electrochemical bio-sensors for micro devices
 - ↳ Novel materials for BioMEMS
 - ↳ MEMS Magnetic circuits
 - ↳ Dielectrophoretic BioMEMS
 - ↳ Microfluidics
 - ↳ Sensors & actuators for catheter systems and minimally invasive surgery
 - ↳ Drug delivery
- ↳ Novel technologies for microsystems and micro devices (e.g. polymer micro-fabrication, doped diamond films, hybrid technologies)

RECENT REPRESENTATIVE PUBLICATIONS

Eg.

- “Optimization of On-Chip Micro-Electromagnets for Biomolecular Separation”
Qasem Ramadan, Victor Samper, Pavel Neuzil, Lesaicherre Marie, Lim Tit Meng, Heng Chew Kiat, Yao Shao Qin, Poenar Daniel Puiu
IEEE Sensors 2002
- “Microfluidic DNA sample preparation by Dielectrophoresis and Electroporation” Qasem Ramadan, Victor Samper, Zhu Liang, Daniel Poenar Puiu, Lim Tit Meng, Heng Chew Kiat, Christina Teh, Chen Yu
Euroensors 2002
- “Microfluidic bead based valve”
Hongmiao Ji, Victor Samper, Wenmiao Shu, Qasem Ramadan, Yu Chen
Euroensors 2002
- “Microfabrication of A Si Mesh Structure Depth Filter”
Yu Chen, Yubo Miao, Victor Samper, Fatimah Bte Mustafa, Qingxin Zhang, Chewkiat Heng, Huijen Lye, Titemeng Lim
MicroTAS 2002, November 2002
- “PCR compatibility of materials incorporated into microfluidic DNA extraction and micro-PCR systems”
Tie Yan, Victor Samper, Chew Kiat HENG, Yubo MIAO, Tit Meng Lim
International Forum on Biochip Technologies 2002, 9-13 November, 2002, Beijing, China
- “Potentiostatic Deposition and Detection of DNA on Conductive Nitrogen Doped Diamond-Like Carbon Film”
A. Zeng, Victor Samper, SN Tan, Daniel Poenar, Titemeng Lim
Transducers '03, June 8-12, 2003, Boston, USA



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MAJOR RESEARCH INTERESTS

1. Si Semiconductor Process Technology
2. Microelectronic Materials Characterization
3. Cu Metallization
4. Chemical Mechanical Planarization
5. Si-Nano finishing
6. Scanning Probe Microscopy

Publications

International Journals: 43

Conferences: 91

US Patent approved: 1

US Patent filed: 6

RECENT REPRESENTATIVE PUBLICATIONS

1. S. BALAKUMAR et al, “Dynamic observations of water-assisted reconstruction on spontaneous Polarization domain ends of Triglycine sulfate (NH₂CH₂COOH) 3.H₂SO₄”, *J. Mater. Chem.*, **1**(2000) 1-6
2. S. BALAKUMAR et al, “Dishing and Nitride Erosion after STI-CMP for 0.18 um Device Using Different Integration Schemes”, *Journal of Electronic Materials*, **Vol. 30** (2001) 1478-1482.
3. S. BALAKUMAR et al, “Stress Effects on the Properties of Copper Layer Employed in the Multi-level Interconnection materials” *19th international VLSI/ULSI Multilevel Interconnections (VMIC) Conference*, 18 - 20 Nov 2002, Singapore.” 177-184
4. S. BALAKUMAR et al , “Evaluation of two types of barrier CMP slurries for Cu/Low *k* materials *2002 Proceedings of 19th International VLSI/ULSI Multilevel Interconnections (VMIC) Conference*, 18 – 20, Nov 2002, Singapore. 381-388
5. S. BALAKUMAR et al, “ Study of Cu-CMP Process Performance for Interconnects Using New Cu Slurries “, *2003 Proceedings of Eight International CMP Planarization for ULSI Multilevel Interconnection Conference (CMP-MIC)*, Singapore 90-94

Patent:

Novel split pads system for CMP to reduce the non-uniformity and dishing
United States Patent 6,248,006.



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MAJOR RESEARCH INTERESTS

Characterisation of semiconductor materials and devices.

Chemical surface analysis, Auger electron spectroscopy, X-ray photoelectron microscopy, time of flight secondary ion mass spectrometry etc.

Applications of scanning capacitance microscopy to semiconductor device characterisation.

Reliability and failure analysis of microelectronic and photonic devices.

Infrared microscopy.

RECENT REPRESENTATIVE PUBLICATIONS

Vanessa Sei-Wei Lim, Yao-Yao Jiang, & Alastair Trigg, Scanning Capacitance Microscopy Study of Si Devices,

Microscopy of Semiconducting Materials XIII, Cambridge UK, 2003,

A combined infrared/visible photoemission microscope.

A D Trigg, Proc. *25th International Symposium on testing & Failure Analysis (ISTFA)*, 457-464, 1999.

Temperature measurement on micromachined IR bolometers using an infrared microscope.

A D Trigg, U. Sridhar, H S Lee & G Karunasiri, Proc. *25th International Symposium on testing & Failure Analysis (ISTFA)*, 189-193, 1999.

Sample preparation for backside failure analysis using infrared photoemission microscopy. Alastair Trigg & Loh Peak Yong, Proc. *25th International Symposium on testing & Failure Analysis (ISTFA)*, 117-124, 1999.

Application of a mercury cadmium telluride focal plane array to semiconductor device manufacturing and reliability. Alastair Trigg, *International Symposium on Photonics and Applications (ISPA) SPIE Vol. 3898* 312-323, 1999.

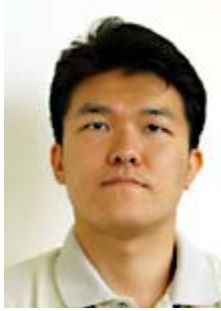
Applications of infrared microscopy to IC and MEMS packaging. Alastair Trigg, Proc. *1st International Workshop on Electronic materials IC packaging and Reliability (EMAP '99)*, 171-181, 1999.

Temperature Mapping of ICs and MEMS Devices Using an Infrared Microscope, A D Trigg. Presented at *Therminic Conference*, Budapest, September 2000

Patents:

A combined infrared and visible light spectroscopic photoemission microscope, A D Trigg. US Patent No 6,121,616 September 2000.

Apparatus and method for image enhancement, A D Trigg. US Patent No 6,433,325, August 2002.



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MAJOR RESEARCH INTERESTS

- Advanced Electronic Packaging
- Wafer Level Integration Technology
- Cu/low-k, Cu/ultra low-k device Flipchip development
- SiMM (Silicon Micro Module) development
- Electroless/Electro Deposition Technology

RECENT REPRESENTATIVE PUBLICATIONS

1. S. W. Yoon and H. M. Lee, "A Thermodynamic Study of Phase Equilibria in the Sn-Bi-Pb Solder System", *CALPHAD*, **Vol.22**, No.,2, pp167-178 (1998).
2. H. M. Lee, S. W. Yoon, B. J. Lee, "Thermodynamic Prediction of Interface Phases at Cu/Solder Joints," *Journal of Electronic Materials*, **Vol.27**, No.11, pp 1161-1166, (1998)
3. S. W. Yoon, B-S. Rho, H. M. Lee, C-U. Kim and B-J. Lee, "Phase Equilibria Analysis of Low Melting Point Solder, Sn-Bi-In System", *Metall. Trans.*, **Vol. 30A**, June, pp.1503-1515(1999).
4. S. W. Yoon and H. M. Lee, "Interfacial Reaction and Growth Behavior of Intermetallic Compounds Formed between Sn-Bi-In-Zn Solder and Cu Substrate", *Scripta Mater.*, **No.40**, No.3, pp.327-332 (1999).
5. S. W. Yoon and H. M. Lee, "Calculation of Surface Tension and Wetting Properties of Sn-Bi-X (X=In, Pb) Solder System", *Scripta Mater.*, **Vol.40**, No.3 pp.297-302(1999).
6. S. W. Yoon, S. H. Hong, C. J. Park and J. T. Moon, "Interfacial reaction and solder joint reliability of Sn-3.5Ag-0.7Cu solders in Lead Frame Chip Scale Package", *Journal of Electronic Materials*, **Vol.29**, No.10, pp. 1233 – 1240, (2000).
7. S. W. Yoon, J. H. Kim, S. W. Jeong and H. M. Lee, "Effect of Under Bump Metallurgy and Reflows on Shear Strength and Microstructure of Joint between Cu Substrate and Sn-36Pb-2Ag Solder Alloy", *Materials Transactions, JIM*, Vol.44, **No.2** , pp.290-297 (2003).
8. J. T. Moon, S. H. Hong, S. W. Yoon, C. J. Park, Y. H. Choi, and Y. H. Koh, "Fabrication Process of Copper Lead Frame Chip Scale Package (LF-CSP)", *Proceeding of the 49th Electronic Components Technology Conference(ECTC)*, San Diego, US, (1999).
9. S. W. Yoon and I. S. Park, "CSP board level reliability testing of Pb-free Sn-Ag-X (X=Cu, In) and polymer-core solder balls," *Proceeding of Pan Pacific SMTA (Surface Mount Technology Association) 2001*, Hawaii, (2001)
10. S. W. Yoon and I.S. Park, "Pb-free technology status in the semiconductor industry", ISS (Industrial Strategy of Semiconductor) 2001, *SEMI(Semiconductor Equipment and Materials International)*, Korea (2001)
11. S. W. Yoon, S.J.Koh, C.S.Shin and H.S.Cheon, "Environmental Issues and Status in Semiconductor Industries," *Proceeding of ISESH(International Semiconductor Environmental Safety and Health) 2001*, Taiwan, (2001)
12. S. W. Yoon, V Kripesh, Wong W. K., Li C. Y., Chen X. T., Gui Dong, I J Rasiah * and M. K. Iyer, "UBM Integrity Studies on Copper/low-k Dielectrics for fine pitch flip chip packaging," *Proceeding of the 53th Electronic Components Technology Conference(ECTC)*, San Diego, US, (2003).



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MAJOR RESEARCH INTERESTS

- High quality on chip RF passive components integration with Cu/SiO₂ and Cu/Low k backend interconnection technology
- High performance MIM capacitor with high k dielectric material for Si RF application
- Silicon base microphotronics device
- Nanocrystalline material and relative device

RECENT REPRESENTATIVE PUBLICATIONS

1. M.B. Yu, Rusli, S.F. Yoon, Z.M.Chen, J. Ahn, Q. Zhang, K. Chew and J. Cui, "Deposition of nanocrystalline cubic silicon carbide films using hot-filament chemical-vapor-deposition method", *J.Appl.Phys.* **Vol. 87**, No. 11, P. 8155-8158 (2000)
2. M. B. Yu, Rusli, S.F. Yoon, S.J. Xu, J. Cui, K. Chew, J. Ahn and Q. Zhang, "Nanocrystalline silicon carbide films synthesized by ECRCVD and its intense visible photoluminescence in room temperature", *Thin Solid Film*, Iss. 377-181 (2000).
3. S.J. Xu, M.B. Yu, Rusli, S.F. Yoon and C.M. Che, "Time-resolved photoluminescence spectra of strong visible light emitting SiC nanocrystalline films on Si deposited by electron cyclotron resonance chemical vapor deposition", *Appl. Phys. Lett.* **Vol. 76, No. 18**, 2550-2552 (2000)
4. G. Lihui, Y. Mingbin, C. Zhen, H. Han and Z. Yi "High Q Multilayer Spiral Inductor on Silicon Chip for 5~6 GHz", IEEE, *Electron Device Letters*, 2002 **Vol.23, No.8**, page(s) 470-472 .



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MAJOR RESEARCH INTERESTS

1. Thermo-mechanical design in advanced packaging technology development
2. Reliability modelling and analysis for microsystems, modules and high density substrate
3. Flip chip technologies
4. Wafer level chip scale packaging and MEMS packaging
5. Stress sensors

RECENT REPRESENTATIVE PUBLICATIONS

1. S-W. R. Lee and X. Zhang (1997) Optimization of temperature profile of the thermal cycling test for PBGA solder joint reliability. *Journal of Surface Mount Technology* **10**, 9-17
2. S-W. R. Lee and X. Zhang (1998) Sensitivity study on material properties for the fatigue life prediction of solder joints under thermal cyclic loading. *Circuit World* **24**, 26-31
3. X. Zhang and S-W. R. Lee (1998) Effects of temperature profile on the life prediction of PBGA solder joints under thermal cycling", *Key Engineering Materials* **145-149**, 1133-1138
4. X. Zhang and S-W. R. Lee (1998) Critical issues in computational modeling and fatigue life analysis for PBGA solder joints. *International Journal of Microcircuits and Electronic Packaging* **21**, 253-261
5. X. Zhang, S-W. R. Lee and Y-H. Pao (2000) A damage evolution model for thermal fatigue of solder joints. *ASME Transaction: Journal of Electronic Packaging* **122**, 200-206
(Received the 2001 JEP Best Paper Award of ASME Transaction: Journal of Electronic Packaging)
6. X. Zhang, C. Q. Cui and K. C. Chan (2000) Analysis of solder joint reliability in flip chip package. *Proceedings of SEMICON@ Singapore 2000 Test, Assembly & Packaging, Singapore*, 193-201
7. X. Zhang, C. Lee, E. H. Wong, M. K. Iyer, P. S. Teo, D. Pinjala and S. Srinivasamurthy (2001) Thermo-mechanical analysis for a multi chip build up substrate based package. *Proceedings of 8th International Symposium on the Physical & Failure Analysis of Integrated Circuits (IPFA 2001), Singapore*, 67-72
8. C. S. Premachandran, X. Zhang, T. C. Chai, V. Samper and T. B. Lim (2001) Study on packaging issues using FEA and experimental verification on Si based capacitive microrelay. *Proceedings of SPIE* **4558**, 226-233
9. S. C. Chong, S. Mohandass, X. Zhang, V. Kripesh and T. C. Chai (2001) Process characterisation of lead free wire bond chip scale package. *Proceedings of International Conference on Advances in Packaging (APACK 2001), Singapore*, 509-516
10. Z.W. Zhong, X. Zhang, B.H. Sim, E. H. Wong, P.S. Teo and M. K. Iyer (2002) Calibration of a piezoresistive stress sensor in (100) silicon test chips. *Proceedings of the 4th Electronics Packaging Technology Conference (EPTC 2002), Singapore*, 323-326
11. X. Zhang and E. H. Wong (2002) Board level reliability enhancement for the transfer molded wafer level CSP. *Proceedings of the 2002 International Conference on Electronic Packaging (2002 ICEP), Japan*, 486-491
12. X. Zhang, S.W.R Lee, K. S. Choi and Y. G. Kim (2002) Computational parametric analyses on the solder joint reliability of bottom leaded plastic (BLP) package. *IEEE Transactions on Advanced Packaging Technologies* **25**, 514-521