

Processing on memory chip delivers speed, size benefits

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Delivering processing capabilities on ReRAM, researchers eye processor elimination, 2x speeds and thinner, lighter electronics.

Software complexity as well as exponential growth in data are driving the quest for faster processing. Current devices and computers transfer data from memory storage to the processor for computation. This takes up separate board space for memory and processing, and the back-and-forth data transfers result in a speed hit.

A team of international scientists have found a way around this challenge by making memory chips perform computing tasks.

This computing memory circuit was developed by Nanyang Technological University, Singapore (NTU Singapore) in collaboration with Germany's RWTH Aachen University and Forschungszentrum Juelich, an interdisciplinary research centre in Europe.

It is built using Redox-based resistive switching random access memory (ReRAM), which is poised to become commercially available. Instead of storing information, NTU Assistant Professor Anupam Chattopadhyay, Professor Rainer Waser from RWTH and Dr Vikas Rana from Forschungszentrum Juelich have shown how ReRAM can be used to process data.

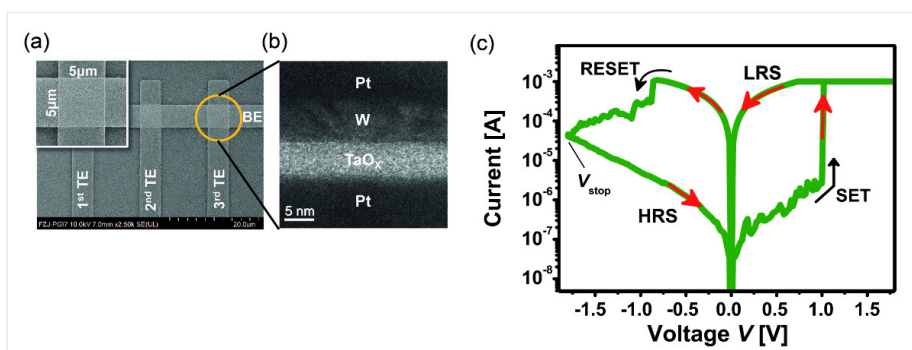


Figure 1: Resistive switching device structures. (a) Scanning electron microscopy image of 1×3 array with the inset showing $5 \times 5 \mu\text{m}^2$ single device; (b) Transmission electron microscopy image of single device cross-section, 7nm thick TaOx switching layer and 13nm thick tungsten ohmic electrode; (c) Typical bipolar operation of SET-RESET switching in DC sweep mode for a single ReRAM ($5 \times 5 \mu\text{m}^2$) device within the 1×3 array. (Credit: Wonjoo Kim, Forschungszentrum Juelich.)

The researchers claim that by making the memory chip perform computing tasks, you can save space by eliminating the processor, leading to thinner, smaller and lighter electronics. Their discovery could also lead to new design possibilities for consumer electronics and wearable technology.

Moreover, the scientists say, the NTU circuit saves time and energy by eliminating data transfers, and it can boost the speed of current processors found in laptops and mobile devices by at least two times.

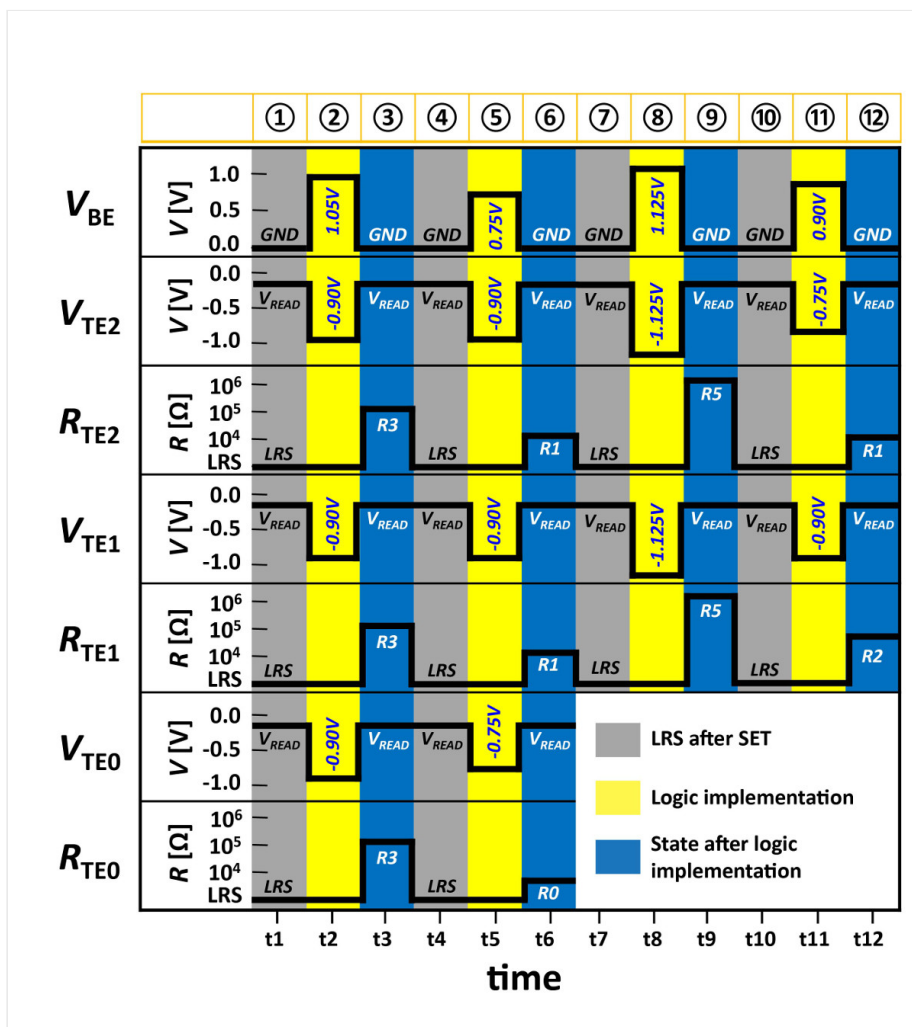


Figure 2: Schematics of operation for applied voltages (V_{TE} , V_{BE}). The grey shows the LRS after SET. The yellow depicts the logic implementations and the blue, the corresponding states after the logic implementation. (Credit: Wonjoo Kim, Forschungszentrum Juelich.)

Detailed description of **figure 2** above: Step 1 is the LRS after initialization and Step 2 is logic implementation. Step 3 is the resistance states

based on Step 2. Step 4 is the LRS after SET and Step 5 implements the RESET for the modulo operation. Step 6 is the corresponding resistance states and Step 7 is the LRS after SET. Step 8 is the logic implementation with adjusted OFFSET and Step 9 is the corresponding resistance states. Step 10 is the LRS after SET. Step 11 is the logic implementation and Step 12 is the corresponding resistance states.

The prototype ReRAM circuit built by Chattopadhyay and his collaborators processes data in three states instead of two using the Ternary number system, instead of the more common Binary.

“This is like having a long conversation with someone through a tiny translator, which is a time-consuming and effort-intensive process,” Chattopadhyay said of using the binary system. “We are now able to increase the capacity of the translator, so it can process data more efficiently.”

Since the ReRAM uses different electrical resistance to store information, it is possible to store the data in an even higher number of states, thereby speeding up computing tasks.

The researchers will work on developing the ReRAM to process more than its current four states, which will lead to great improvements of computing speeds as well as to test its performance in actual computing scenarios.

The properties of ReRAM like long-term storage capacity, low energy usage and the ability to be produced at the nanoscale level have drawn many semiconductor companies to research in this area.

The team is now looking to engage with such industry partners to leverage ReRAM-based ternary computing.