Embargoed until 11.00am, 12 Jan 2007

Reg. No. 200604393R

FACT SHEET

About the aRfic-NTU scholarships

The investment from aRfic will create thirty postgraduate scholarships for NTU students. Each scholarship provides the student with $2,000 per month for 24 months.

The scholarships are for students pursuing a Master of Engineering (MEng) programme at NTU School of Electrical and Electronic Engineering. Students awarded the scholarships will work on one or more of the four projects identified by NTU and aRfic.

Applications for the scholarships are for the next class intake in July 2007. Applications open from February 2007.

About the projects

The projects have been jointly identified by NTU and aRfic.

1. Project 1: Advanced Characterization and Modeling of CMOS devices

   Most of the commercially available RF transistor model is usually developed only for a single transistor size. This causes problems to the circuit designers as the RF models provided by the foundries are not fully scalable. More specifically, the transistors may not be of the desired dimensions required by the circuit designer. In order to obtain that RF model for a specific transistor size, modeling engineers will require fabricating several different sizes of transistor and develop the respective RF models again. This method of generating of the RF model is time consuming and will increase the design cycle time of RF circuits.

   This project will aim to develop a scalable RF model so that circuit designers can design their circuits with greater flexibility.

2. Project 2: RF Interconnects for RFIC Design and Applications

   The frequency-dependent nature of the interconnects must be considered in RFIC design and applications. However, frequency-dependent parameters are currently not supported in most circuit simulators.

   In this project, frequency-independent equivalent circuit models are proposed to incorporate those frequency-dependent effects.

   The final objective of this project is to setup fully scalable lumped or even distributed circuit models of on-wafer interconnect which could be incorporated into commercial simulators for RF circuit design. This is a new and huge market.

3. Project 3: R&D on Electronic Design Automation for RFIC Design

   As designs get smaller and more complex, coupled with increasing shorter product life-cycles, design companies are faced with the need to meet the short design schedule and critical time-to-market.

   This project aims to develop an advanced electronic design kit, which is basically an integration of all technology files that enables designers to create, simulate, optimize and verify their designs from front-end to back-end using foundry-specific processes. This kit will have the following benefits: Save Setup Time; Cut-Short Design Cycle and Time-to-Market; Reduced Cost.

4. Project 4: Design of Low-Power Optical Transceiver ICs

   Data traffic continues to grow at an explosive pace. Leading Internet Service Providers (ISR) reported on bandwidth that is doubling on their backbones at approximately every six to nine months. Today, Service providers are demanding data rate exceeding 10-Gb/s.

   In this research project, the design of fully integrated ultra high-speed low-power clock and data recovery (CDR) circuits, TIA, AGC, photo-detectors and DEMUX/DEMUX in CMOS for synchronous optical network (SONET) applications will be explored and developed. Despite the aggressive device scaling in CMOS technology, these circuits which will be realized in CMOS process still face significant high frequency design and speed constraints. When it comes to complying with the stringent jitter requirements posed by the standards, CMOS circuits have to work harder than its GaAs or SiGe counterparts to overcome the limitations due to the high-frequency parasitics. Extensive research work must be carried out at all fronts

related to the CMOS circuits in order to obtain a total solution to the problems currently faced by the designers.

*** END ***